



UPD784031GC-8BT-A
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Arrow Electronics, Inc
9201 East Dry Creek Road
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16/8-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD784031 is a product of the μ PD784038 sub-series in the 78K/IV series. It contains various peripheral hardware such as RAM, I/O ports, 8-bit resolution A/D and D/A converters, timers, serial interface, and interrupt functions, as well as a high-speed, high-performance CPU.

The μ PD784031 is a ROM-less product of the μ PD784035 and μ PD784036.

For specific functions and other detailed information, consult the following user's manual.

This manual is required reading for design work.

μ PD784038, 784038Y Sub-Series User's Manual, Hardware : U11316E
78K/IV Series User's Manual, Instruction : U10905E

Features

- Pin-compatible with the μ PD78234, μ PD784026, and μ PD784038Y sub-series
- Minimum instruction execution time: 125 ns (at 32 MHz)
- Number of I/O ports: 46
- Serial interface: 3 channels
UART/IOE (3-wire serial I/O): 2 channels
CSI (3-wire serial I/O, 2-wire serial I/O): 1 channel
- PWM outputs: 2
- Timer/counters
16-bit timer/counter \times 3 units
16-bit timer \times 1 unit
- Standby function
HALT/STOP/IDLE mode
- Clock frequency division function
- Watchdog timer: 1 channel
- A/D converter: 8-bit resolution \times 8 channels
- D/A converter: 8-bit resolution \times 2 channels
- Power supply voltage: $V_{DD} = 2.7$ to 5.5 V

Applications

LBP, automatic-focusing camera, PPC, printer, electronic typewriter, air conditioner, electronic musical instruments, cellular telephone, etc.

Ordering Information

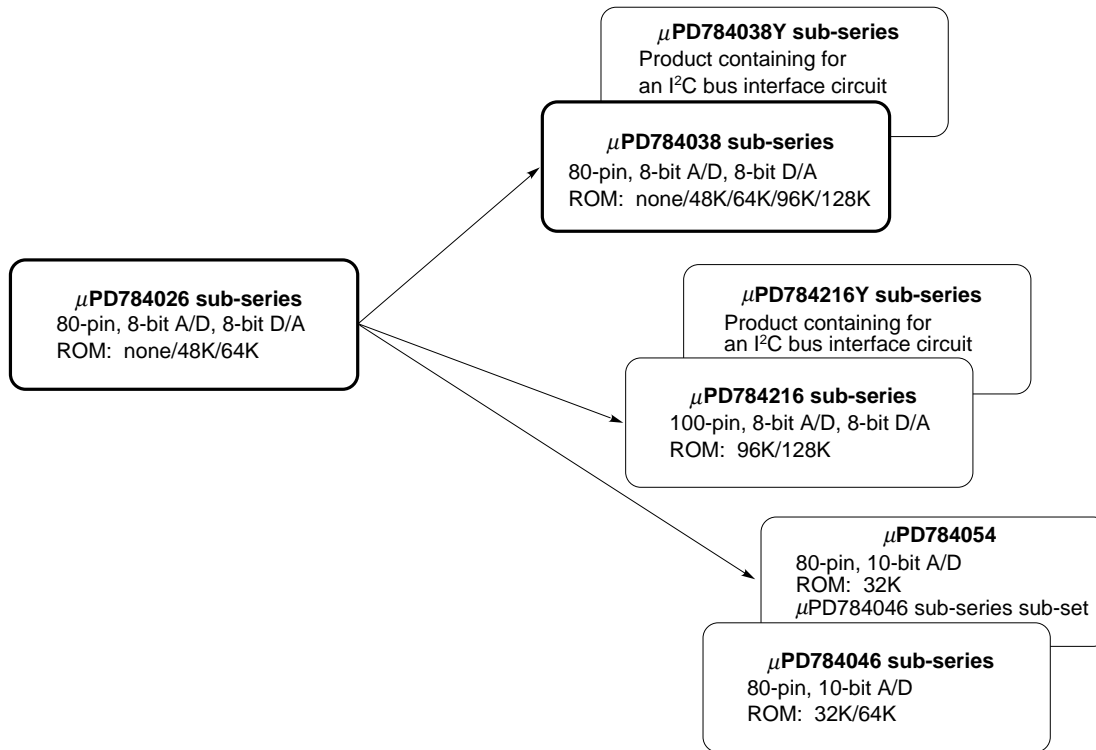
| Part number | Package | Internal ROM (bytes) | Internal RAM (bytes) |
|------------------------|--|-------------------------|-------------------------|
| μ PD784031GC-3B9 | 80-pin plastic QFP (14 \times 14 \times 2.7 mm) | None | 2 048 |
| ★ μ PD784031GC-8BT | 80-pin plastic QFP (14 \times 14 \times 1.4 mm) | None | 2 048 |
| μ PD784031GK-BE9 | 80-pin plastic TQFP (fine pitch) (12 \times 12 mm) | None | 2 048 |

The information in this document is subject to change without notice.

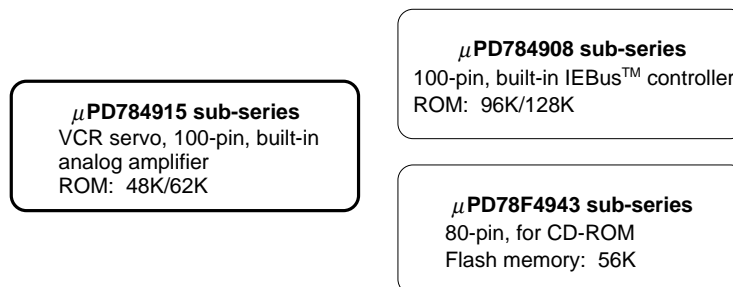
★ 78K/IV Series Product Development Diagram

- : Product under mass production
- : Product under development

Standard Products Development



ASSP Development



Functions

| Item | | Function | | |
|--|----------------------------|---|--|---|
| Number of basic instructions (mnemonics) | | 113 | | |
| General-purpose register | | 8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping) | | |
| Minimum instruction execution time | | 125 ns/250 ns/500 ns/1 000 ns (at 32 MHz) | | |
| Internal memory | ROM | None | | |
| | RAM | 2 048 bytes | | |
| Memory space | | Program and data: 1M byte | | |
| I/O ports | Total | 46 | | |
| | Input | 8 | | |
| | Input/output | 34 | | |
| | Output | 4 | | |
| Additional function pins ^{Note} | Pins with pull-up resistor | 32 | | |
| | LED direct drive outputs | 8 | | |
| | Transistor direct drive | 8 | | |
| Real-time output ports | | 4 bits × 2, or 8 bits × 1 | | |
| Timer/counter | | Timer/counter 0: (16 bits) | Timer register × 1 Capture register × 1 Compare register × 2 | Pulse output capability • Toggle output • PWM/PPG output • One-shot pulse output |
| | | Timer/counter 1: (8/16 bits) | Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1 | Pulse output capability • Real-time output (4 bits × 2) |
| | | Timer/counter 2: (8/16 bits) | Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1 | Pulse output capability • Toggle output • PWM/PPG output |
| | | Timer 3 (8/16 bits) | Timer register × 1 Compare register × 1 | |
| PWM outputs | | 12-bit resolution × 2 channels | | |
| Serial interface | | UART/IOE (3-wire serial I/O) : 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O, 2-wire serial I/O): 1 channel | | |
| A/D converter | | 8-bit resolution × 8 channels | | |
| D/A converter | | 8-bit resolution × 2 channels | | |
| Watchdog timer | | 1 channel | | |
| Standby | | HALT/STOP/IDLE mode | | |
| Interrupt | Hardware source | 23 (16 internal, 7 external (sampling clock variable input: 1)) | | |
| | Software source | BRK instruction, BRKCS instruction, operand error | | |
| | Nonmaskable | 1 internal, 1 external | | |
| | Maskable | 15 internal, 6 external | | |
| | | <ul style="list-style-type: none"> • 4-level programmable priority • 3 operation statuses: vectored interrupt, macro service, context switching | | |
| Supply voltage | | V _{DD} = 2.7 to 5.5 V | | |
| Package | | 80-pin plastic QFP (14 × 14 × 2.7 mm) 80-pin plastic QFP (14 × 14 × 1.4 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm) | | |

Note Additional function pins are included in the I/O pins.

CONTENTS

| | | |
|-------|---|----|
| 1. | DIFFERENCES BETWEEN μ PD784038 SUB-SERIES | 6 |
| 2. | MAIN DIFFERENCES BETWEEN μ PD784038, μ PD784038Y, μ PD784026, AND μ PD78234 SUB-SERIES | 7 |
| 3. | PIN CONFIGURATION (TOP VIEW) | 8 |
| 4. | SYSTEM CONFIGURATION EXAMPLE (PPC) | 10 |
| 5. | BLOCK DIAGRAM | 11 |
| 6. | LIST OF PIN FUNCTIONS | 12 |
| 6.1 | Port Pins | 12 |
| 6.2 | Non-Port Pins | 13 |
| 6.3 | I/O Circuits for Pins and Handling of Unused Pins | 15 |
| 7. | CPU ARCHITECTURE | 18 |
| 7.1 | Memory Space | 18 |
| 7.2 | CPU Registers | 20 |
| 7.2.1 | General-purpose registers | 20 |
| 7.2.2 | Control registers | 21 |
| 7.2.3 | Special function registers (SFRs) | 22 |
| 8. | PERIPHERAL HARDWARE FUNCTIONS | 27 |
| 8.1 | Ports | 27 |
| 8.2 | Clock Generator | 28 |
| 8.3 | Real-Time Output Port | 30 |
| 8.4 | Timers/Counters | 31 |
| 8.5 | PWM Output (PWM0, PWM1) | 33 |
| 8.6 | A/D Converter | 34 |
| 8.7 | D/A Converter | 35 |
| 8.8 | Serial Interface | 36 |
| 8.8.1 | Asynchronous serial interface/three-wire serial I/O (UART/IOE) | 37 |
| 8.8.2 | Synchronous serial interface (CSI) | 39 |
| 8.9 | Edge Detection Function | 40 |
| 8.10 | Watchdog Timer | 40 |
| 9. | INTERRUPT FUNCTION | 41 |
| 9.1 | Interrupt Source | 41 |
| 9.2 | Vectored Interrupt | 43 |
| 9.3 | Context Switching | 44 |
| 9.4 | Macro Service | 44 |
| 9.5 | Examples of Macro Service Applications | 45 |

| | |
|---|----|
| 10. LOCAL BUS INTERFACE | 47 |
| 10.1 Memory Expansion | 47 |
| 10.2 Memory Space | 48 |
| 10.3 Programmable Wait | 49 |
| 10.4 Pseudo-Static RAM Refresh Function | 49 |
| 10.5 Bus Hold Function | 49 |
| 11. STANDBY FUNCTION | 50 |
| 12. RESET FUNCTION | 51 |
| 13. INSTRUCTION SET | 52 |
| ★ 14. ELECTRICAL CHARACTERISTICS | 57 |
| 15. PACKAGE DRAWINGS..... | 77 |
| ★ 16. RECOMMENDED SOLDERING CONDITIONS | 80 |
| APPENDIX A DEVELOPMENT TOOLS | 82 |
| APPENDIX B RELATED DOCUMENTS | 84 |

1. DIFFERENCES BETWEEN μPD784038 SUB-SERIES

The only difference between the μPD784031, μPD784035, μPD784036, μPD784037, and μPD784038 is their capacity of internal memory.

The μPD78P4038 is produced by replacing the masked ROM in the μPD784035, μPD784036, μPD784037, or μPD784038 with 128K-byte one-time PROM or EPROM. Table 1-1 shows the differences between these products.

Table 1-1. Differences between the μPD784038 Sub-Series

| Product Item | μPD784031 | μPD784035 | μPD784036 | μPD784037 (under development) | μPD784038 (under development) | μPD78P4038 |
|--------------|---|---------------------------|---------------------------|----------------------------------|----------------------------------|---|
| Internal ROM | None | 48K bytes (masked ROM) | 64K bytes (masked ROM) | 96K bytes (masked ROM) | 128K bytes (masked ROM) | 128K bytes (one-time PROM or EPROM) |
| Internal RAM | 2 048 bytes | | | 3 584 bytes | 4 352 bytes | |
| Package | 80-pin plastic QFP (14 × 14 × 2.7 mm) 80-pin plastic QFP (14 × 14 × 1.4 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm) | | | | | 80-pin ceramic WQFN (14 × 14 mm) |

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2. MAIN DIFFERENCES BETWEEN μPD784038, μPD784038Y, μPD784026, AND μPD78234 SUB-SERIES

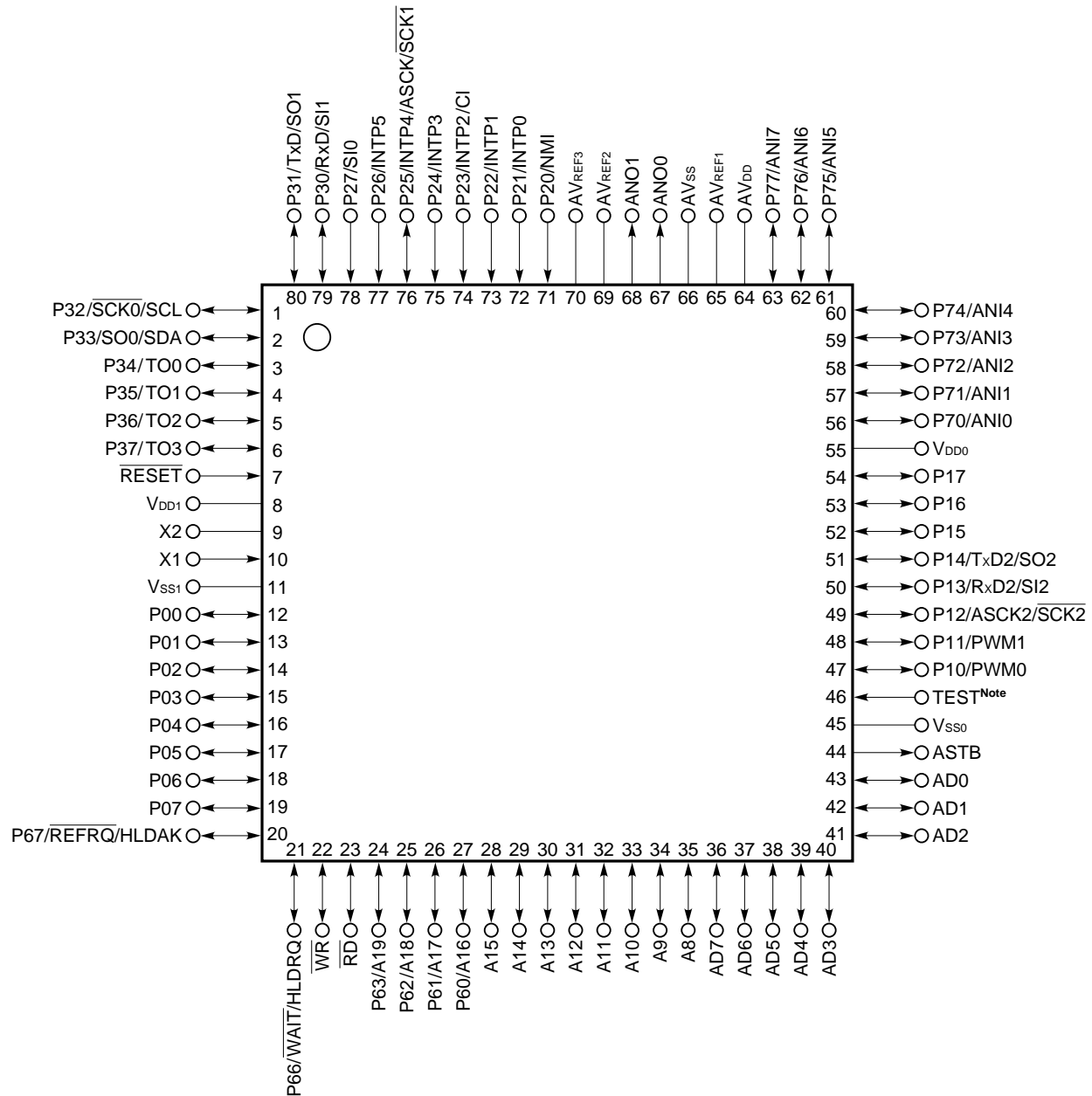
| Series | | μPD784038 sub-series μPD784038Y sub-series | μPD784026 sub-series | μPD78234 sub-series |
|--|-------------------|---|---|---|
| Item | | | | |
| Number of basic instructions (mnemonics) | | 113 | | 65 |
| Minimum instruction execution time | | 125 ns (at 32 MHz) | 160 ns (at 25 MHz) | 333 ns (at 12 MHz) |
| Memory space (program/data) | | 1M byte in total | | 64K bytes/1M byte |
| Timer/counter | | 16-bit timer/counter × 1 8/16-bit timer/counter × 2 8/16-bit timer × 1 | | 16-bit timer/counter × 1 8-bit timer/counter × 2 8-bit timer × 1 |
| Clock output function | | Available | | Unavailable |
| Watchdog timer | | Available | | Unavailable |
| Serial interface | | UART/IOE (3-wire serial I/O) × 2 channels CSI (3-wire serial I/O, 2-wire serial I/O, I ² C bus ^{Note}) × 1 channel | UART/IOE (3-wire serial I/O) × 2 channels CSI (3-wire serial I/O, SBI) × 1 channel | UART × 1 channel CSI (3-wire serial I/O, SBI) × 1 channel |
| Interrupt | Context switching | Available | | Unavailable |
| | Priority | 4 levels | | 2 levels |
| Standby function | | 3 modes (HALT, STOP, IDLE) | | 2 modes (HALT, STOP) |
| Operation clock switching | | Selectable from f _{xx} /2, f _{xx} /4, f _{xx} /8, or f _{xx} /16 | | Fixed to f _{xx} /2 |
| Pin functions | MODE pin | Unavailable | | To specify ROM-less mode (always in the high level for the μPD78233 or μPD78237) |
| | TEST pin | Pin for testing the device Low level during ordinary use | | Unavailable |
| Package | | 80-pin plastic QFP (14 × 14 × 2.7 mm) 80-pin plastic QFP (14 × 14 × 1.4 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm) 80-pin ceramic WQFN (14 × 14 mm): for the μPD78P4038 and μPD78P4038Y only | 80-pin plastic QFP (14 × 14 × 2.7 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm): for the μPD784021 only 80-pin ceramic WQFN (14 × 14 mm): for the μPD78P4026 only | 80-pin plastic QFP (14 × 14 × 2.7 mm) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1 150 × 1 150 mil) 94-pin ceramic WQFN (20 × 20 mm): for the μPD78P238 only |

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Note For the μPD784038Y sub-series only.

3. PIN CONFIGURATION (TOP VIEW)

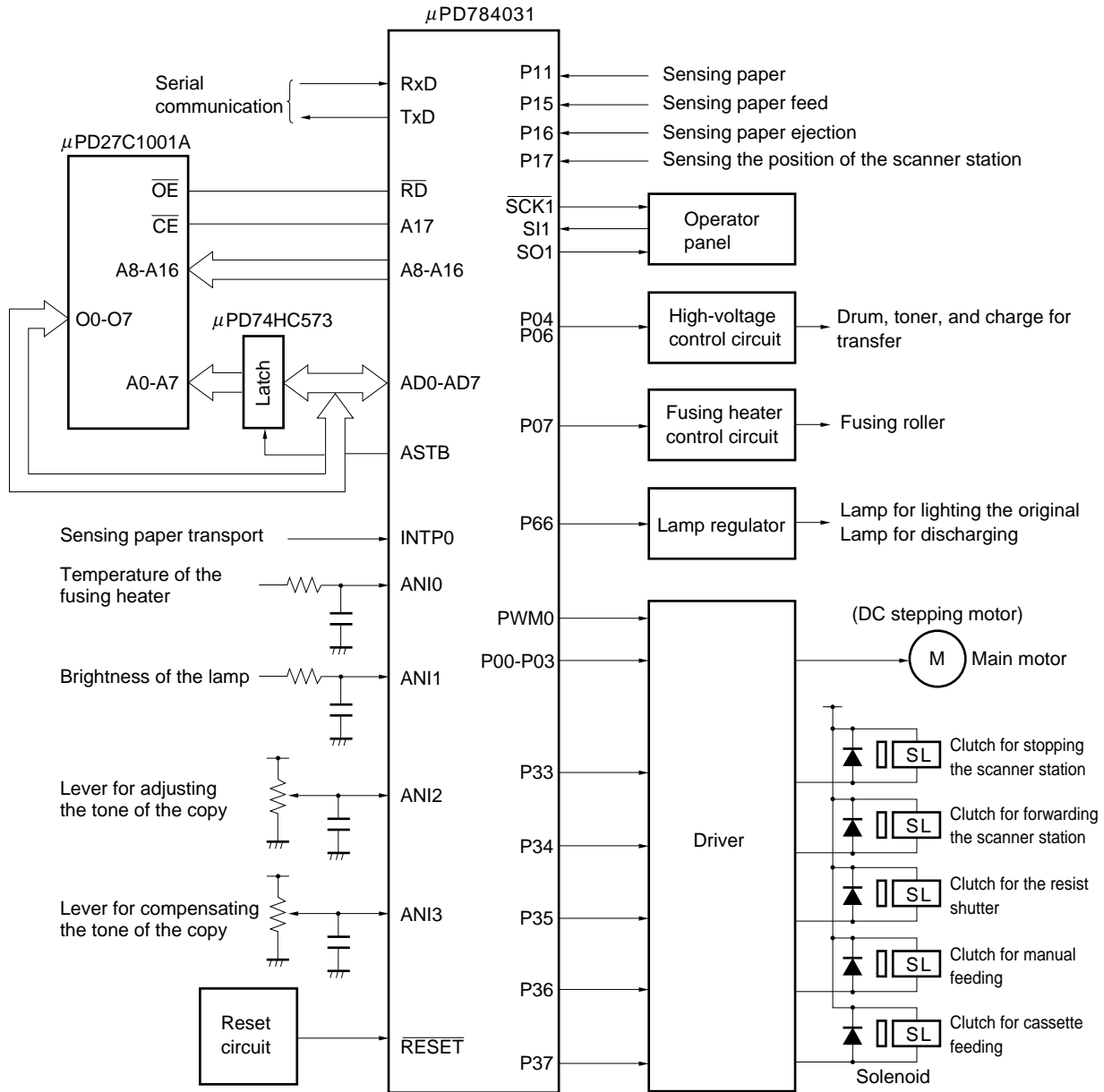
- 80-pin plastic QFP (14 × 14 × 2.7 mm)
μPD784031GC-3B9
- ★ • 80-pin plastic QFP (14 × 14 × 1.4 mm)
μPD784031GC-8BT
- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD784031GK-BE9



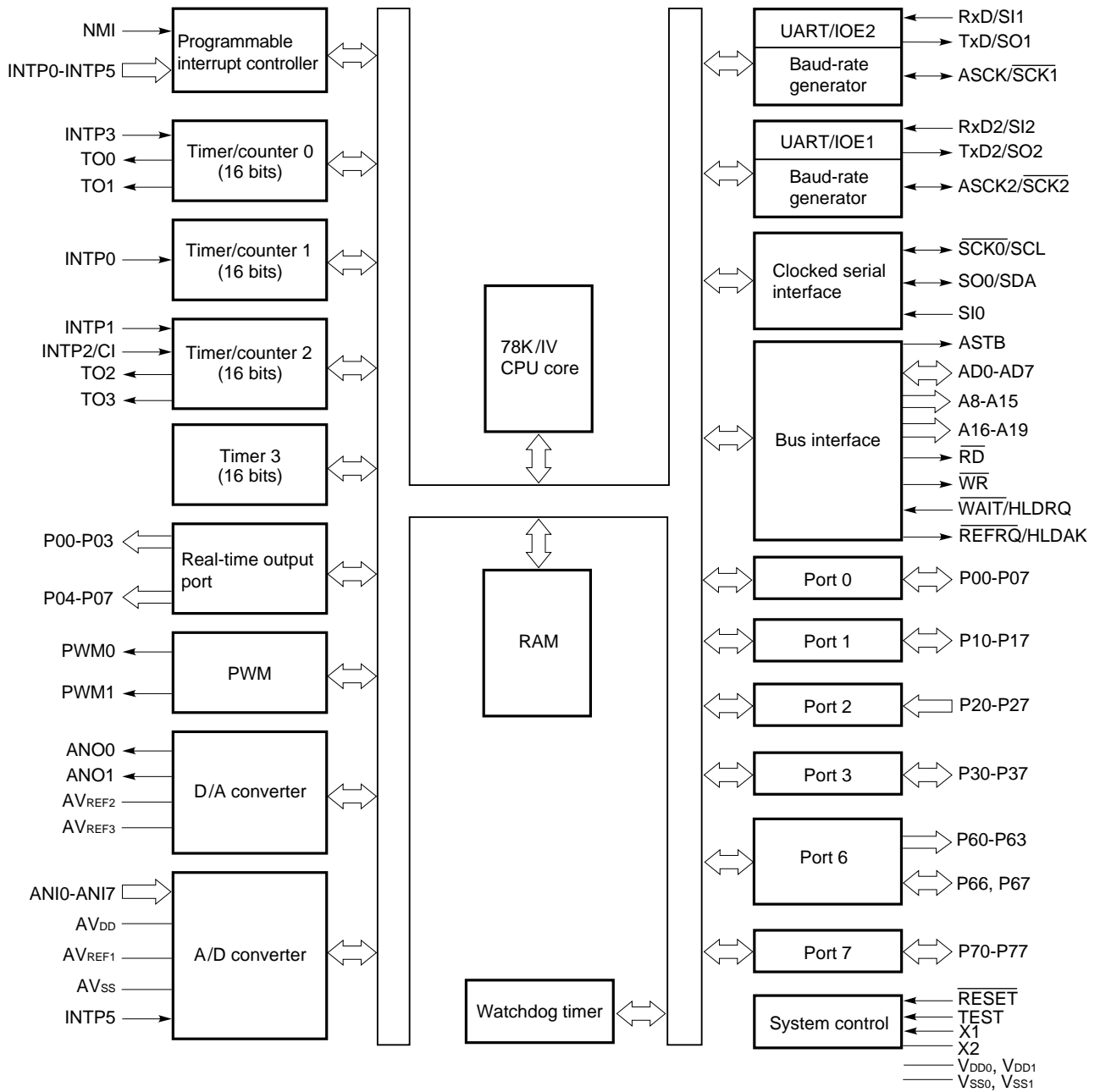
Note Connect the TEST pin to V_{SS0} directly.

| | | | |
|-------------------------|------------------------------|-------------------------------------|---------------------------------|
| A8-A19 | : Address bus | P70-P77 | : Port 7 |
| AD0-AD7 | : Address/data bus | PWM0, PWM1 | : Pulse width modulation output |
| ANI0-ANI7 | : Analog input | \overline{RD} | : Read strobe |
| ANO0, ANO1 | : Analog output | \overline{REFRQ} | : Refresh request |
| ASCK, ASCK2 | : Asynchronous serial clock | \overline{RESET} | : Reset |
| ASTB | : Address strobe | RxD, RxD2 | : Receive data |
| AV _{DD} | : Analog power supply | $\overline{SCK0-SCK2}$ | : Serial clock |
| AV _{REF1-REF3} | : Reference voltage | SCL | : Serial clock |
| AV _{SS} | : Analog ground | SDA | : Serial data |
| CI | : Clock input | SI0-SI2 | : Serial input |
| HLD _{AK} | : Hold acknowledge | SO0-SO2 | : Serial output |
| HLD _{RQ} | : Hold request | TEST | : Test |
| INTP0-INTP5 | : Interrupt from peripherals | TO0-TO3 | : Timer output |
| NMI | : Non-maskable interrupt | TxD, TxD2 | : Transmit data |
| P00-P07 | : Port 0 | V _{DD0} , V _{DD1} | : Power supply |
| P10-P17 | : Port 1 | V _{SS0} , V _{SS1} | : Ground |
| P20-P27 | : Port 2 | \overline{WAIT} | : Wait |
| P30-P37 | : Port 3 | \overline{WR} | : Write strobe |
| P60-P63, P66, P67 | : Port 6 | X1, X2 | : Crystal |

4. SYSTEM CONFIGURATION EXAMPLE (PPC)



5. BLOCK DIAGRAM



6. LIST OF PIN FUNCTIONS

6.1 Port Pins

| Pin | I/O | Dual-function | Function |
|---------|-------|-----------------|--|
| P00-P07 | I/O | - | <p>Port 0 (P0):</p> <ul style="list-style-type: none"> • 8-bit I/O port. • Functions as a real-time output port (4 bits × 2). • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive a transistor. |
| P10 | I/O | PWM0 | <p>Port 1 (P1):</p> <ul style="list-style-type: none"> • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive LED. |
| P11 | | PWM1 | |
| P12 | | ASCK2/SCK2 | |
| P13 | | RxD2/SI2 | |
| P14 | | TxD2/SO2 | |
| P15-P17 | | - | |
| P20 | Input | NMI | <p>Port 2 (P2):</p> <ul style="list-style-type: none"> • 8-bit input-only port. • P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of the pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits). • The P25/INTP4/ASCK/SCK1 pin functions as the SCK1 output pin by CSIM1. |
| P21 | | INTP0 | |
| P22 | | INTP1 | |
| P23 | | INTP2/C1 | |
| P24 | | INTP3 | |
| P25 | | INTP4/ASCK/SCK1 | |
| P26 | | INTP5 | |
| P27 | | SI0 | |
| P30 | I/O | RxD/SI1 | <p>Port 3 (P3):</p> <ul style="list-style-type: none"> • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. |
| P31 | | TxD/SO1 | |
| P32 | | SCK0/SCL | |
| P33 | | SO0/SDA | |
| P34-P37 | | TO0-TO3 | |
| P60-P63 | I/O | A16-A19 | <p>Port 6 (P6):</p> <ul style="list-style-type: none"> • P60 to P63 are an output-only port. • Inputs and outputs can be specified bit by bit for pins P66 and P67. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. |
| P66 | | WAIT/HLDRQ | |
| P67 | | REFRQ/HLDAK | |
| P70-P77 | I/O | ANI0-ANI7 | <p>Port 7 (P7):</p> <ul style="list-style-type: none"> • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. |

6.2 Non-Port Pins (1/2)

| Pin | I/O | Dual-function | Function | |
|---------------------------|--------|-------------------------------------|---|---|
| TO0-TO3 | Output | P34-P37 | Timer output | |
| CI | Input | P23/INTP2 | Input of a count clock for timer/counter 2 | |
| RxD | Input | P30/SI1 | Serial data input (UART0) | |
| RxD2 | | P13/SI2 | Serial data input (UART2) | |
| TxD | Output | P31/SO1 | Serial data output (UART0) | |
| TxD2 | | P14/SO2 | Serial data output (UART2) | |
| ASCK | Input | P25/INTP4/ $\overline{\text{SCK1}}$ | Baud rate clock input (UART0) | |
| ASCK2 | | P12/ $\overline{\text{SCK2}}$ | Baud rate clock input (UART2) | |
| SDA | I/O | P33/SO0 | Serial data I/O (2-wire serial I/O) | |
| SI0 | Input | P27 | Serial data input (3-wire serial I/O0) | |
| SI1 | | P30/RxD | Serial data input (3-wire serial I/O1) | |
| SI2 | | P13/RxD2 | Serial data input (3-wire serial I/O2) | |
| SO0 | Output | P33/SDA | Serial data output (3-wire serial I/O0) | |
| SO1 | | P31/TxD | Serial data output (3-wire serial I/O1) | |
| SO2 | | P14/TxD2 | Serial data output (3-wire serial I/O2) | |
| $\overline{\text{SCK0}}$ | I/O | P32/SCL | Serial clock I/O (3-wire serial I/O0) | |
| $\overline{\text{SCK1}}$ | | P25/INTP4/ASCK | Serial clock I/O (3-wire serial I/O1) | |
| $\overline{\text{SCK2}}$ | | P12/ASCK2 | Serial clock I/O (3-wire serial I/O2) | |
| SCL | | P32/ $\overline{\text{SCK0}}$ | Serial clock I/O (2-wire serial I/O) | |
| NMI | Input | P20 | External interrupt request | - |
| INTP0 | | P21 | | <ul style="list-style-type: none"> Input of a count clock for timer/counter 1 Capture/trigger signal for CR11 or CR12 |
| INTP1 | | P22 | | <ul style="list-style-type: none"> Input of a count clock for timer/counter 2 Capture/trigger signal for CR22 |
| INTP2 | | P23/CI | | <ul style="list-style-type: none"> Input of a count clock for timer/counter 2 Capture/trigger signal for CR21 |
| INTP3 | | P24 | | <ul style="list-style-type: none"> Input of a count clock for timer/counter 0 Capture/trigger signal for CR02 |
| INTP4 | | P25/ASCK/ $\overline{\text{SCK1}}$ | | - |
| INTP5 | | P26 | | Input of a conversion start trigger for A/D converter |
| AD0-AD7 | I/O | - | Time multiplexing address/data bus (for connecting external memory) | |
| A8-A15 | Output | - | High-order address bus (for connecting external memory) | |
| A16-A19 | Output | P60-P63 | High-order address bus during address expansion (for connecting external memory) | |
| $\overline{\text{RD}}$ | Output | - | Strobe signal output for reading the contents of external memory | |
| $\overline{\text{WR}}$ | Output | - | Strobe signal output for writing on external memory | |
| $\overline{\text{WAIT}}$ | Input | P66/HLDRQ | Wait signal insertion | |
| $\overline{\text{REFRQ}}$ | Output | P67/HLDAK | Refresh pulse output to external pseudo static memory | |
| HLDRQ | Input | P66/ $\overline{\text{WAIT}}$ | Input of bus hold request | |
| HLDAK | Output | P67/ $\overline{\text{REFRQ}}$ | Output of bus hold response | |
| ASTB | Output | - | Latch timing output of time multiplexing address (A0-A7) (for connecting external memory) | |

6.2 Non-port pins (2/2)

| Pin | I/O | Dual-function | Function |
|----------------------|--------|---------------|---|
| RESET | Input | - | Chip reset |
| X1 | Input | - | Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.) |
| X2 | - | | |
| ANI0-ANI7 | Input | P70-P77 | Analog voltage inputs for the A/D converter |
| ANO0, ANO1 | Output | - | Analog voltage inputs for the D/A converter |
| AVREF1 | - | - | Application of A/D converter reference voltage |
| AVREF2, AVREF3 | | | Application of D/A converter reference voltage |
| AVDD | | | Positive power supply for the A/D converter |
| AVSS | | | Ground for the A/D converter |
| ★ VDD0 Note 1 | | | Positive power supply of the port part |
| ★ VDD1 Note 1 | | | Positive power supply except for the port part |
| ★ VSS0 Note 2 | | | Ground of the port part |
| ★ VSS1 Note 2 | | | Ground except for the port part |
| TEST | | | Directly connect to VSS0. (The TEST pin is for the IC test.) |

Notes 1. The potential of the VDD0 pin must be equal to that of the VDD1 pin.

2. The potential of the VSS0 pin must be equal to that of the VSS1 pin.

6.3 I/O Circuits for Pins and Handling of Unused Pins

Table 6-1 describes the types of I/O circuits for pins and the handling of unused pins.

Figure 6-1 shows the configuration of these various types of I/O circuits.

★

Table 6-1. Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

| Pin | I/O circuit type | I/O | Recommended connection method for unused pins | | |
|---------------------|------------------|------------------------|--|------|--|
| P00-P07 | 5-H | I/O | Input state : To be connected to V _{DD0} Output state: To be left open | | |
| P10/PWM0 | | | | | |
| P11/PWM1 | | | | | |
| P12/ASCK2/SCK2 | | | | | |
| P13/RxD2/SI2 | | | | | |
| P14/TxD2/SO2 | | | | | |
| P15-P17 | 2 | Input | To be connected to V _{DD0} or V _{SS0} | | |
| P20/NMI | | | | | |
| P21/INTP0 | | | | | |
| P22/INTP1 | | | | 2-C | To be connected to V _{DD0} |
| P23/INTP2/CI | | | | | |
| P24/INTP3 | | | | | |
| P25/INTP4/ASCK/SCK1 | | | | | |
| P26/INTP5 | 2-C | Input | To be connected to V _{DD0} | | |
| P27/SI0 | | | | | |
| P30/RxD/SI1 | 5-H | I/O | Input state : To be connected to V _{DD0} Output state: To be left open | | |
| P31/TxD/SO1 | | | | | |
| P32/SCK0/SCL | 10-B | | | | |
| P33/SO0/SDA | | | | | |
| P34/TO0-P37/TO3 | 5-H | Output ^{Note} | To be left open | | |
| AD0-AD7 | | | | | |
| A8-A15 | | | | | |
| P60/A16-P63/A19 | | | | | |
| RD | | | | | |
| WR | | I/O | Input state: To be connected to V _{DD0} Output state: To be left open | | |
| P66/WAIT/HLDRQ | | | | | |
| P67/REFRQ/HLDAK | | | | | |
| P70/ANI0-P77/ANI7 | | | | 20-A | Input state : To be connected to V _{DD0} or V _{SS0} Output state: To be left open |
| ANO0, ANO1 | | | | | |
| ASTB | 4-B | Output | To be left open | | |

Note These pins function as output-only pins depending on the internal circuit, though their I/O type is 5-H.

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Table 6-1. Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

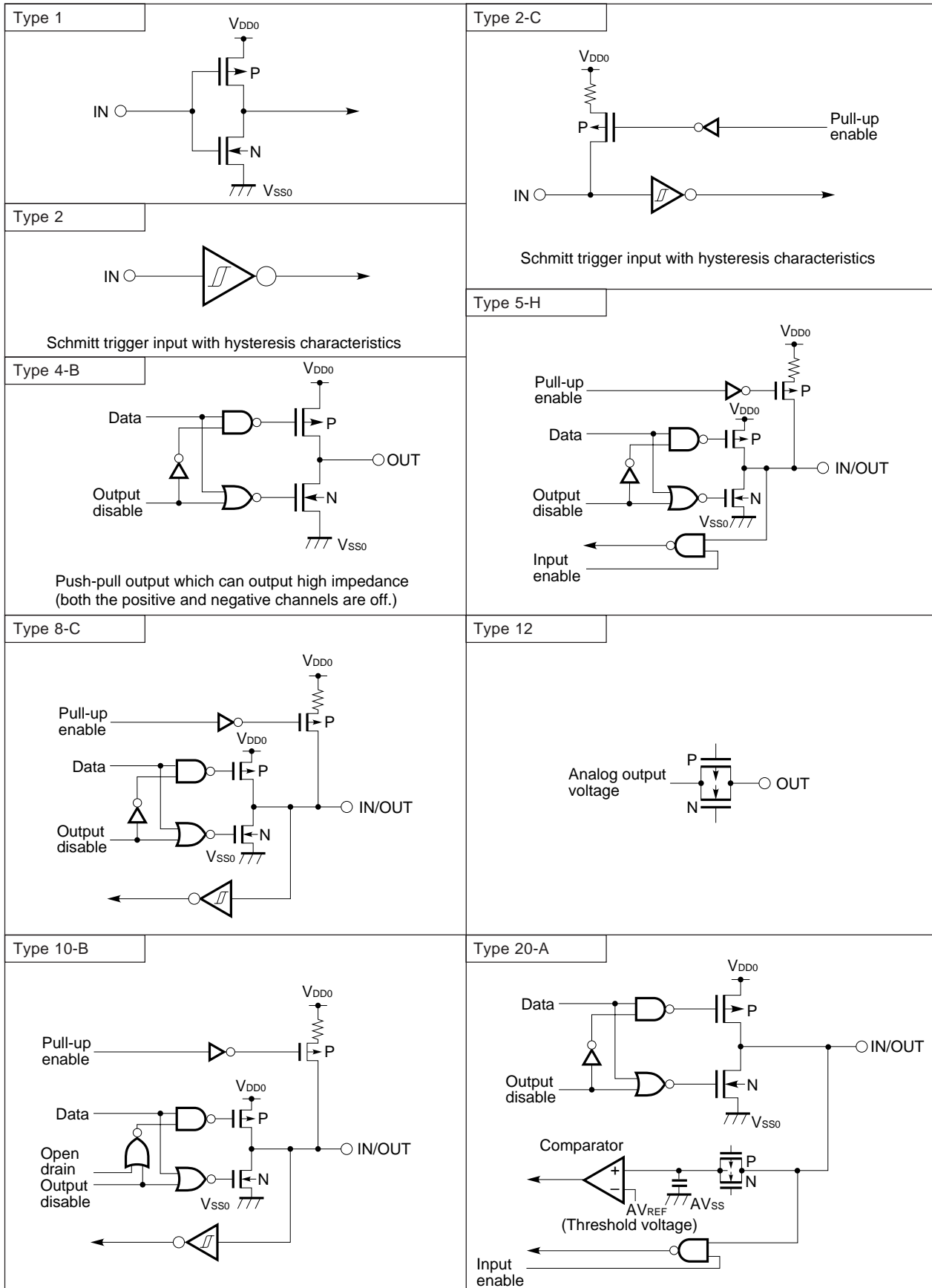
| Pin | I/O circuit type | I/O | Recommended connection method for unused pins |
|--|------------------|-------|---|
| RESET | 2 | Input | - |
| TEST | 1-A | | To be connected to V _{SS0} directly |
| AV _{REF1} -AV _{REF3} | - | | To be connected to V _{SS0} |
| AV _{SS} | | | |
| AV _{DD} | | | To be connected to V _{DD0} |

Caution When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to V_{DD0} through a resistor of 10 to 100 kilohms (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

Remark Since type numbers are consistent in the 78K series, those numbers are not always serial in each product. (Some circuits are not included.)

★

Figure 6-1. I/O Circuits for Pins



7. CPU ARCHITECTURE

7.1 Memory Space

A 1M-byte memory space can be accessed. By using a LOCATION instruction, the mode for mapping internal data areas (special function registers and internal RAM) can be selected. A LOCATION instruction must always be executed after a reset, and can be used only once.

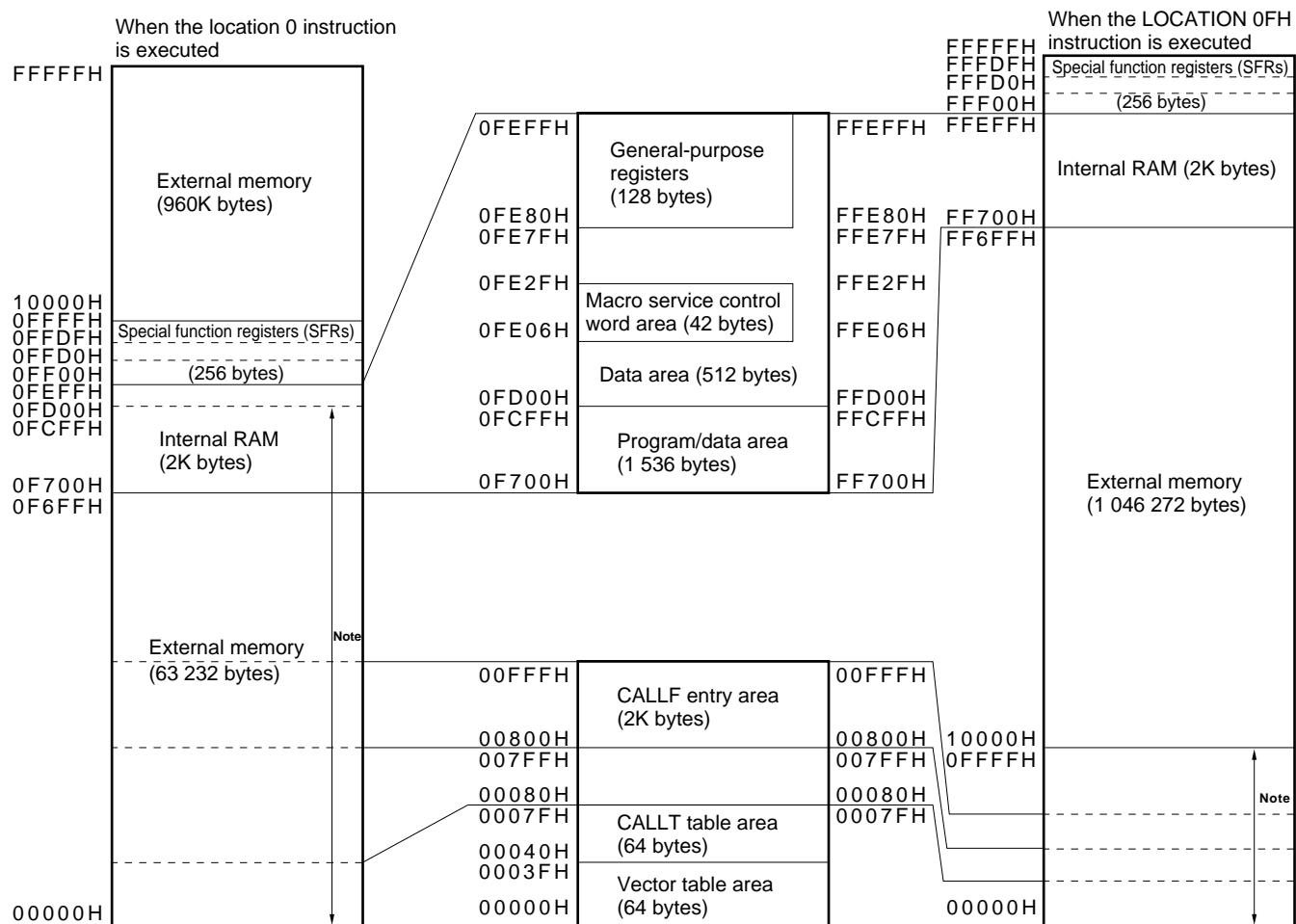
(1) When the LOCATION 0 instruction is executed

Internal data areas are mapped to 0F700H-0FFFFH.

(2) When the LOCATION 0FH instruction is executed

Internal data areas are mapped to FF700H-FFFFFFH.

Figure 7-1. μ PD784031 Memory Map



Note Base area, or entry area based on a reset or interrupt. Internal RAM is excluded in the case of a reset.

7.2 CPU Registers

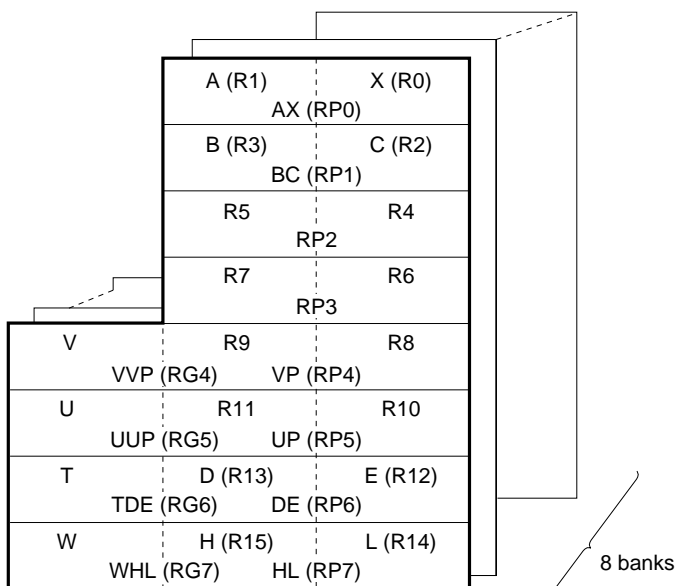
7.2.1 General-purpose registers

A set of general-purpose registers consists of sixteen general-purpose 8-bit registers. Two 8-bit general-purpose registers can be combined to form a 16-bit general-purpose register. Moreover, four 16-bit general-purpose registers, when combined with an 8-bit register for address extension, can be used as 24-bit address specification registers.

Eight banks of this register set are provided. The user can switch between banks by software or the context switching function.

General-purpose registers other than the V, U, T, and W registers used for address extension are mapped onto internal RAM.

Figure 7-2. General-Purpose Register Format



The character strings enclosed in parentheses represent absolute names.

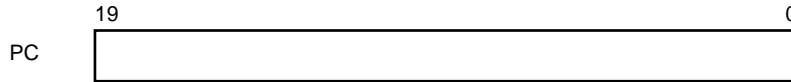
Caution By setting the RSS bit of PSW to 1, R4, R5, R6, R7, RP2, and RP3 can be used as the X, A, C, B, AX, and BC registers, respectively. However, this function must be used only when using programs for the 78K/III series.

7.2.2 Control registers

(1) Program counter (PC)

This register is a 20-bit program counter. The program counter is automatically updated by program execution.

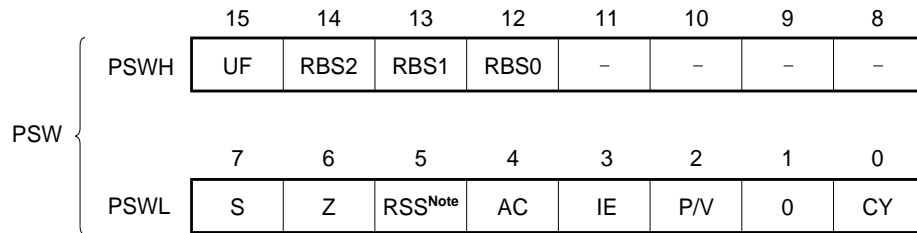
Figure 7-3. Format of Program Counter (PC)



(2) Program Status Word (PSW)

This register holds the CPU state. The program status word is automatically updated by program execution.

Figure 7-4. Format of Program Status Word (PSW)

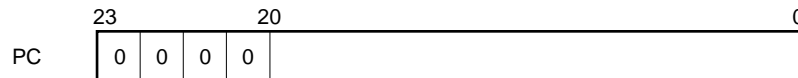


Note This flag is used to maintain compatibility with the 78K/III series. This flag must be set to 0 when programs for the 78K/III series are being used.

(3) Stack pointer (SP)

This register is a 24-bit pointer for holding the start address of the stack. The high-order 4 bits must be set to 0.

Figure 7-5. Format of Stack Pointer (SP)



7.2.3 Special function registers (SFRs)

The special function registers are registers with special functions such as mode registers and control registers for built-in peripheral hardware. The special function registers are mapped onto the 256-byte space between 0FF00H and 0FFFFH^{Note}.

Note Applicable when the LOCATION 0 instruction is executed. FFF00H-FFFFFH when the LOCATION 0FH instruction is executed.

Caution Never attempt to access addresses in this area where no SFR is allocated. Otherwise, the μPD784031 may be placed in the deadlock state. The deadlock state can be cleared only by a reset.

Table 7-1 lists the special function registers (SFRs). The titles of the table columns are explained below.

- Abbreviation Symbol used to represent a built-in SFR. The abbreviations listed in the table are reserved words for the NEC assembler (RA78K4). The C compiler (CC78K4) allows the abbreviations to be used as sfr variables with the #pragma sfr command.
- R/W Indicates whether each SFR allows read and/or write operations.
 - R/W : Allows both read and write operations.
 - R : Allows read operations only.
 - W : Allows write operations only.
- Manipulatable bits Indicates the maximum number of bits that can be manipulated whenever an SFR is manipulated. An SFR that supports 16-bit manipulation can be described in the sfrp operand. For address specification, an even-numbered address must be specified.
 - An SFR that supports 1-bit manipulation can be described in a bit manipulation instruction.
- When reset Indicates the state of each register when $\overline{\text{RESET}}$ is applied.

Table 7-1. Special Function Registers (SFRs) (1/4)

| Address ^{Note} | Special function register (SFR) name | | Abbreviation | R/W | Manipulatable bits | | | When reset |
|-------------------------|--|--------------------------|--------------|-------|--------------------|--------|-----------|------------|
| | | | | | 1 bit | 8 bits | 16 bits | |
| 0FF00H | Port 0 | | P0 | R/W | o | o | - | Undefined |
| 0FF01H | Port 1 | | P1 | | o | o | - | |
| 0FF02H | Port 2 | | P2 | R | o | o | - | 00H |
| 0FF03H | Port 3 | | P3 | R/W | o | o | - | |
| 0FF06H | Port 6 | | P6 | | o | o | - | Undefined |
| 0FF07H | Port 7 | | P7 | o | o | - | | |
| 0FF0EH | | Port 0 buffer register L | P0L | o | o | - | Undefined | |
| 0FF0FH | Port 0 buffer register H | | P0H | o | o | - | | |
| 0FF10H | Compare register (timer/counter 0) | | CR00 | - | - | o | Undefined | |
| 0FF12H | Capture/compare register (timer/counter 0) | | CR01 | - | - | o | | |
| 0FF14H | Compare register L (timer/counter 1) | | CR10 | CR10W | - | o | o | Undefined |
| 0FF15H | Compare register H (timer/counter 1) | | - | | - | - | - | |
| 0FF16H | Capture/compare register L (timer/counter 1) | | CR11 | CR11W | - | o | o | Undefined |
| 0FF17H | Capture/compare register H (timer/counter 1) | | - | | - | - | - | |
| 0FF18H | Compare register L (timer/counter 2) | | CR20 | CR20W | - | o | o | Undefined |
| 0FF19H | Compare register H (timer/counter 2) | | - | | - | - | - | |
| 0FF1AH | Capture/compare register L (timer/counter 2) | | CR21 | CR21W | - | o | o | Undefined |
| 0FF1BH | Capture/compare register H (timer/counter 2) | | - | | - | - | - | |
| 0FF1CH | Compare register L (timer 3) | | CR30 | CR30W | - | o | o | Undefined |
| 0FF1DH | Compare register H (timer 3) | | - | | - | - | - | |
| 0FF20H | Port 0 mode register | | PM0 | o | o | - | FFH | |
| 0FF21H | Port 1 mode register | | PM1 | o | o | - | | |
| 0FF23H | Port 3 mode register | | PM3 | o | o | - | 00H | |
| 0FF26H | Port 6 mode register | | PM6 | o | o | - | | |
| 0FF27H | Port 7 mode register | | PM7 | o | o | - | 00H | |
| 0FF2EH | Real-time output port control register | | RTPC | o | o | - | | |
| 0FF30H | Capture/compare control register 0 | | CRC0 | - | o | - | 10H | |
| 0FF31H | Timer output control register | | TOC | o | o | - | 00H | |
| 0FF32H | Capture/compare control register 1 | | CRC1 | - | o | - | 10H | |
| 0FF33H | Capture/compare control register 2 | | CRC2 | - | o | - | | |

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F000H is added to each address.

Table 7-1. Special Function Registers (SFRs) (2/4)

| Address ^{Note} | Special function register (SFR) name | Abbreviation | | R/W | Manipulatable bits | | | When reset | | |
|-------------------------|--|--------------|-------|-----|--------------------|--------|---------|------------|---|-----|
| | | | | | 1 bit | 8 bits | 16 bits | | | |
| 0FF36H | Capture register (timer/counter 0) | CR02 | | R | - | - | o | 0000H | | |
| 0FF38H | Capture register L (timer/counter 1) | CR12 | CR12W | | - | o | o | | | |
| 0FF39H | Capture register H (timer/counter 1) | - | | | - | - | | | | |
| 0FF3AH | Capture register L (timer/counter 2) | CR22 | CR22W | | - | o | o | | | |
| 0FF3BH | Capture register H (timer/counter 2) | - | | | - | - | | | | |
| 0FF41H | Port 1 mode control register | PMC1 | | R/W | o | o | - | 00H | | |
| 0FF43H | Port 3 mode control register | PMC3 | | | o | o | - | | | |
| 0FF4EH | Register for optional pull-up resistor | PUO | | | o | o | - | | | |
| 0FF50H | Timer register 0 | TM0 | | R | - | - | o | 0000H | | |
| 0FF51H | | | | | - | - | | | | |
| 0FF52H | Timer register 1 | TM1 | TM1W | | - | o | o | | | |
| 0FF53H | | - | | | - | - | | | | |
| 0FF54H | Timer register 2 | TM2 | TM2W | | - | o | o | | | |
| 0FF55H | | - | | | - | - | | | | |
| 0FF56H | Timer register 3 | TM3 | TM3W | | - | o | o | | | |
| 0FF57H | | - | | | - | - | | | | |
| 0FF5CH | Prescaler mode register 0 | PRM0 | | | R/W | - | o | | - | 11H |
| 0FF5DH | Timer control register 0 | TMC0 | | | | o | o | | - | 00H |
| 0FF5EH | Prescaler mode register 1 | PRM1 | | - | | o | - | 11H | | |
| 0FF5FH | Timer control register 1 | TMC1 | | o | | o | - | 00H | | |
| 0FF60H | D/A conversion value setting register 0 | DACS0 | | - | | o | - | 00H | | |
| 0FF61H | D/A conversion value setting register 1 | DACS1 | | - | | o | - | | | |
| 0FF62H | D/A converter mode register | DAM | | o | | o | - | 03H | | |
| 0FF68H | A/D converter mode register | ADM | | o | | o | - | 00H | | |
| 0FF6AH | A/D conversion result register | ADCR | | R | - | o | - | Undefined | | |
| 0FF70H | PWM control register | PWMC | | R/W | o | o | - | 05H | | |
| 0FF71H | PWM prescaler register | PWPR | | | - | o | - | 00H | | |
| 0FF72H | PWM modulo register 0 | PWM0 | | | - | - | o | Undefined | | |
| 0FF74H | PWM modulo register 1 | PWM1 | | | - | - | o | | | |
| 0FF7DH | One-shot pulse output control register | OSPC | | | o | o | - | 00H | | |
| 0FF80H | I ² C bus control register | IICC | | | o | o | - | | | |
| 0FF81H | Prescaler mode register for serial clock | SPRM | | | - | o | - | 04H | | |
| 0FF82H | Synchronous serial interface mode register | CSIM | | | o | o | - | 00H | | |

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 7-1. Special Function Registers (SFRs) (3/4)

| Address ^{Note 1} | Special function register (SFR) name | Abbreviation | R/W | Manipulatable bits | | | When reset | |
|---------------------------|---|--------------|-----|--------------------|---------------------|---------|------------|---|
| | | | | 1 bit | 8 bits | 16 bits | | |
| 0FF84H | Synchronous serial interface mode register 1 | CSIM1 | R/W | o | o | - | 00H | |
| 0FF85H | Synchronous serial interface mode register 2 | CSIM2 | | o | o | - | | |
| 0FF86H | Serial shift register | SIO | | - | o | - | | |
| 0FF88H | Asynchronous serial interface mode register | ASIM | | o | o | - | | |
| 0FF89H | Asynchronous serial interface mode register 2 | ASIM2 | | o | o | - | | |
| 0FF8AH | Asynchronous serial interface status register | ASIS | R | o | o | - | Undefined | |
| 0FF8BH | Asynchronous serial interface status register 2 | ASIS2 | | o | o | - | | |
| 0FF8CH | Serial receive buffer: UART0 | RXB | W | - | o | - | Undefined | |
| | Serial transmission shift register: UART0 | TXS | | - | o | - | | |
| | Serial shift register: IOE1 | SIO1 | | R/W | - | o | | - |
| 0FF8DH | Serial receive buffer: UART2 | RXB2 | R | - | o | - | Undefined | |
| | Serial transmission shift register: UART2 | TXS2 | W | - | o | - | | |
| | Serial shift register: IOE2 | SIO2 | R/W | - | o | - | | |
| 0FF90H | Baud rate generator control register | BRGC | R | - | o | - | 00H | |
| 0FF91H | Baud rate generator control register 2 | BRGC2 | | - | o | - | | |
| 0FFA0H | External interrupt mode register 0 | INTM0 | | o | o | - | | |
| 0FFA1H | External interrupt mode register 1 | INTM1 | | o | o | - | | |
| 0FFA4H | Sampling clock selection register | SCS0 | | - | o | - | | |
| 0FFA8H | In-service priority register | ISPR | R | o | o | - | 80H | |
| 0FFAAH | Interrupt mode control register | IMC | R/W | o | o | - | | |
| 0FFACH | Interrupt mask register 0L | MK0L | | MK0 | o | o | | o |
| 0FFADH | Interrupt mask register 0H | MK0H | | | o | o | | |
| 0FFAEH | Interrupt mask register 1L | MK1L | | o | o | - | | |
| 0FFC0H | Standby control register | STBC | | - | ^{Note 2} o | - | | |
| 0FFC2H | Watchdog timer mode register | WDM | | - | ^{Note 2} o | - | | |
| 0FFC4H | Memory expansion mode register | MM | | o | o | - | | |
| 0FFC5H | Hold mode register | HLDM | | o | o | - | | |
| 0FFC6H | Clock output mode register | CLOM | | o | o | - | | |
| 0FFC7H | Programmable wait control register 1 | PWC1 | | - | o | - | AAH | |
| 0FFC8H | Programmable wait control register 2 | PWC2 | - | - | o | AAAAH | | |

Notes 1. Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F000H is added to each address.

2. A write operation can be performed only with special instructions MOV STBC,#byte and MOV WDM,#byte. Other instructions cannot perform a write operation.

Table 7-1. Special Function Registers (SFRs) (4/4)

| Address ^{Note} | Special function register (SFR) name | Abbreviation | R/W | Manipulatable bits | | | When reset |
|-------------------------|--|--------------|-----|--------------------|--------|---------|------------|
| | | | | 1 bit | 8 bits | 16 bits | |
| 0FFCCH | Refresh mode register | RFM | R/W | o | o | - | 00H |
| 0FFCDH | Refresh area specification register | RFA | | o | o | - | |
| 0FFCFH | Oscillation settling time specification register | OSTS | | - | o | - | |
| 0FFD0H- 0FFDFH | External SFR area | - | | o | o | - | - |
| 0FFE0H | Interrupt control register (INTP0) | PIC0 | R/W | o | o | - | 43H |
| 0FFE1H | Interrupt control register (INTP1) | PIC1 | | o | o | - | |
| 0FFE2H | Interrupt control register (INTP2) | PIC2 | | o | o | - | |
| 0FFE3H | Interrupt control register (INTP3) | PIC3 | | o | o | - | |
| 0FFE4H | Interrupt control register (INTC00) | CIC00 | | o | o | - | |
| 0FFE5H | Interrupt control register (INTC01) | CIC01 | | o | o | - | |
| 0FFE6H | Interrupt control register (INTC10) | CIC10 | | o | o | - | |
| 0FFE7H | Interrupt control register (INTC11) | CIC11 | | o | o | - | |
| 0FFE8H | Interrupt control register (INTC20) | CIC20 | | o | o | - | |
| 0FFE9H | Interrupt control register (INTC21) | CIC21 | | o | o | - | |
| 0FFEAH | Interrupt control register (INTC30) | CIC30 | | o | o | - | |
| 0FFEBH | Interrupt control register (INTP4) | PIC4 | | o | o | - | |
| 0FFECH | Interrupt control register (INTP5) | PIC5 | | o | o | - | |
| 0FFEDH | Interrupt control register (INTAD) | ADIC | | o | o | - | |
| 0FFEEH | Interrupt control register (INTSER) | SERIC | | o | o | - | |
| 0FFEFH | Interrupt control register (INTSR) | SRIC | | o | o | - | |
| | Interrupt control register (INTCSI1) | CSIIC1 | | o | o | - | |
| 0FFF0H | Interrupt control register (INTST) | STIC | | o | o | - | |
| 0FFF1H | Interrupt control register (INTCSI) | CSIIC | | o | o | - | |
| 0FFF2H | Interrupt control register (INTSER2) | SERIC2 | | o | o | - | |
| 0FFF3H | Interrupt control register (INTSR2) | SRIC2 | | o | o | - | |
| | Interrupt control register (INTCSI2) | CSIIC2 | | o | o | - | |
| 0FFF4H | Interrupt control register (INTST2) | STIC2 | | o | o | - | |

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F000H is added to each address.

8. PERIPHERAL HARDWARE FUNCTIONS

8.1 Ports

The ports shown in Figure 8-1 are provided to enable the application of wide-ranging control. Table 8-1 lists the functions of the ports. For the inputs to port 0 to port 6, a built-in pull-up resistor can be specified by software.

Figure 8-1. Port Configuration

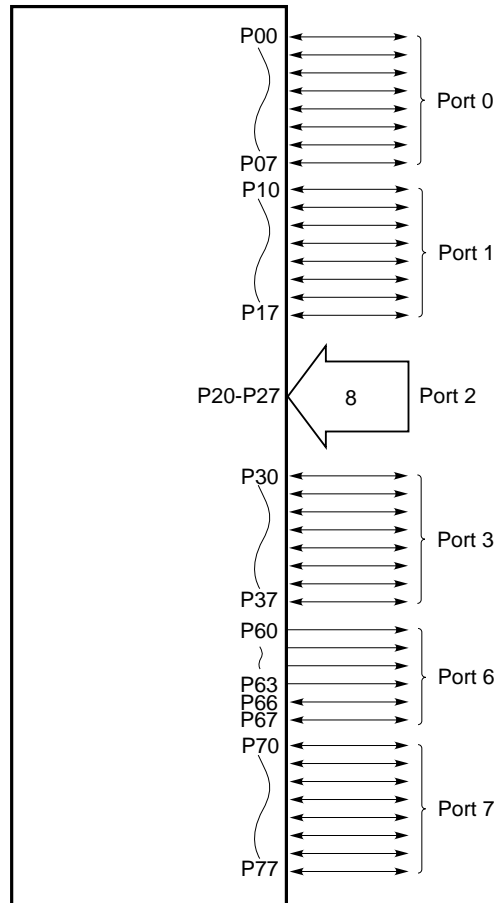


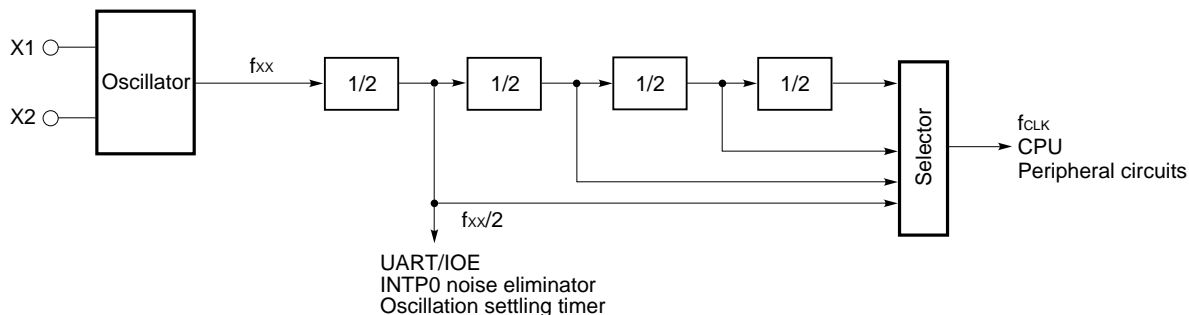
Table 8-1. Port Functions

| Port name | Pin | Function | Pull-up specification by software |
|-----------|----------|---|---|
| Port 0 | P00-P07 | <ul style="list-style-type: none"> • Bit-by-bit input/output setting supported • Operable as 4-bit real-time outputs (P00-P03, P04-P07) • Capable of driving transistors | Specified as a batch for all pins placed in input mode. |
| Port 1 | P10-P17 | <ul style="list-style-type: none"> • Bit-by-bit input/output setting supported • Capable of driving LEDs | Specified as a batch for all pins placed in input mode. |
| Port 2 | P20-P27 | • Input port | Specified for the 6 bits (P22-P27) as a batch. |
| Port 3 | P30-P37 | • Bit-by-bit input/output setting supported | Specified as a batch for all pins placed in input mode. |
| Port 6 | P60-P63 | • Output-only port | Specified as a batch for all pins placed in input mode. |
| | P66, P67 | • Bit-by-bit input/output setting supported | |
| Port 7 | P70-P77 | • Bit-by-bit input/output setting supported | - |

8.2 Clock Generator

A circuit for generating the clock signal required for operation is provided. The clock generator includes a frequency divider; low current consumption can be achieved by operating at a lower internal frequency when high-speed operation is not necessary.

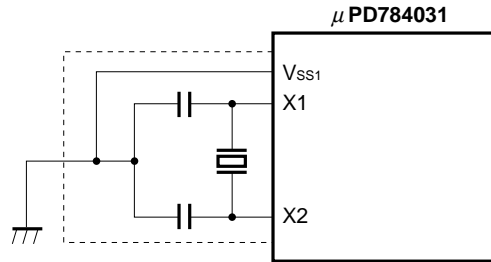
Figure 8-2. Block Diagram of Clock Generator



Remark f_{xx} : Oscillator frequency or external clock input
 f_{CLK} : Internal operating frequency

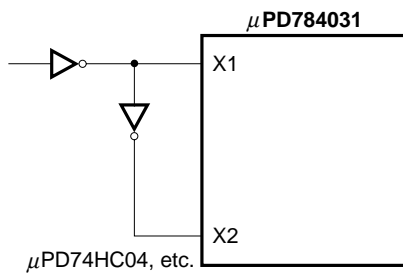
Figure 8-3. Examples of Using Oscillator

(1) Crystal/ceramic oscillation

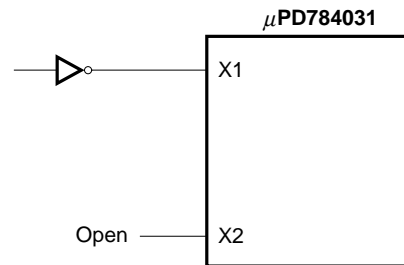


(2) External clock

- When EXTC bit of OSTS = 1



- When EXTC bit of OSTS = 0



Caution When using the clock generator, to avoid problems caused by influences such as stray capacitance, run all wiring within the area indicated by the dotted lines according to the following rules:

- Minimize the wiring length.
- Wires must never cross other signal lines.
- Wires must never run near a line carrying a large varying current.
- The grounding point of the capacitor of the oscillator circuit must always be at the same potential as V_{SS1}. Never connect the capacitor to a ground pattern carrying a large current.
- Never extract a signal from the oscillator circuit.

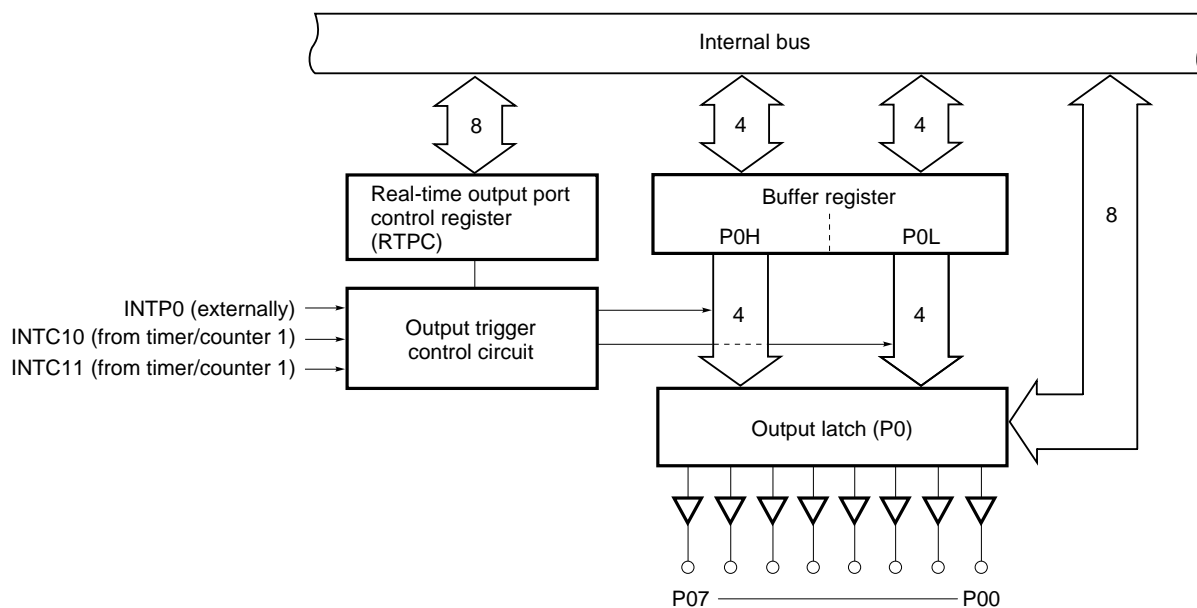
8.3 Real-Time Output Port

The real-time output port outputs data stored in the buffer, synchronized with a timer/counter 1 match interrupt or external interrupt. Thus, pulse output that is free of jitter can be obtained.

Therefore, the real-time output port is best suited to applications (such as open-loop control over stepping motors) where an arbitrary pattern is output at arbitrary intervals.

As shown in Figure 8-4, the real-time output port is built around port 0 and the port 0 buffer register (P0H, P0L).

Figure 8-4. Block Diagram of Real-Time Output Port



8.4 Timers/Counters

Three timer/counter units and one timer unit are incorporated.

Moreover, seven interrupt requests are supported, allowing these units to function as seven timer/counter units.

Table 8-2. Timer/Counter Operation

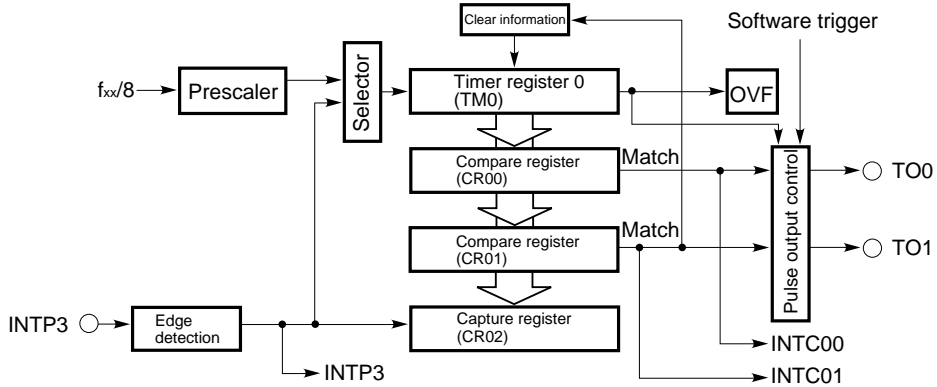
| Name | | Timer/counter 0 | Timer/counter 1 | Timer/counter 2 | Timer 3 |
|-------------------|---------------------------------------|-----------------|-----------------|-----------------|---------|
| Item | | | | | |
| Count pulse width | 8 bits | - | o | o | o |
| | 16 bits | o | o | o | o |
| Operating mode | Interval timer | 2ch | 2ch | 2ch | 1ch |
| | External event counter | o | o | o | - |
| | One-shot timer | - | - | o | - |
| Function | Timer output | 2ch | - | 2ch | - |
| | Toggle output | o | - | o | - |
| | PWM/PPG output | o | - | o | - |
| | One-shot pulse output ^{Note} | o | - | - | - |
| | Real-time output | - | o | - | - |
| | Pulse width measurement | 1 input | 1 input | 2 inputs | - |
| | Number of interrupt requests | 2 | 2 | 2 | 1 |

Note The one-shot pulse output function makes the level of a pulse output active by software, and makes the level of a pulse output inactive by hardware (interrupt request signal).

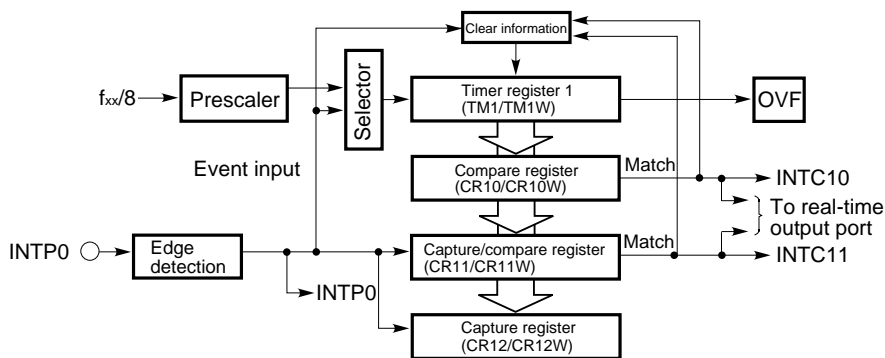
Note that this function differs from the one-shot timer function of timer/counter 2.

Figure 8-5. Timer/Counter Block Diagram

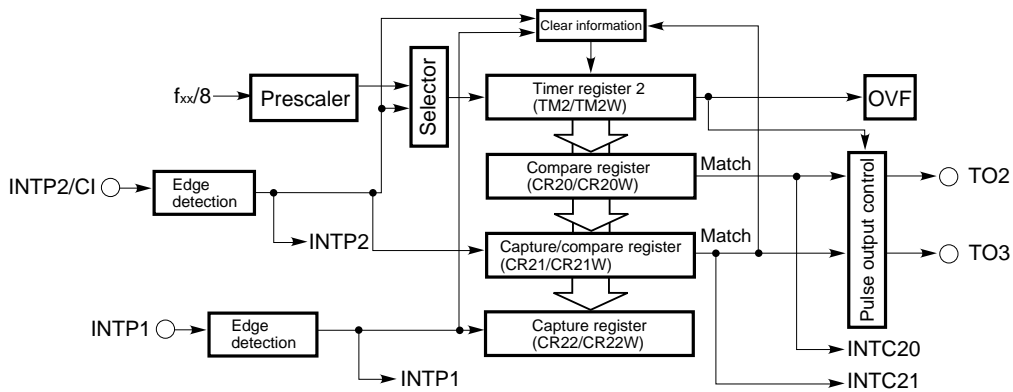
Timer/counter 0



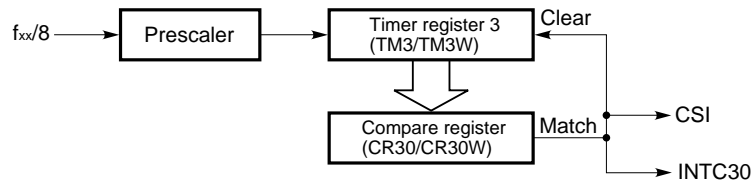
Timer/counter 1



Timer/counter 2



Timer 3

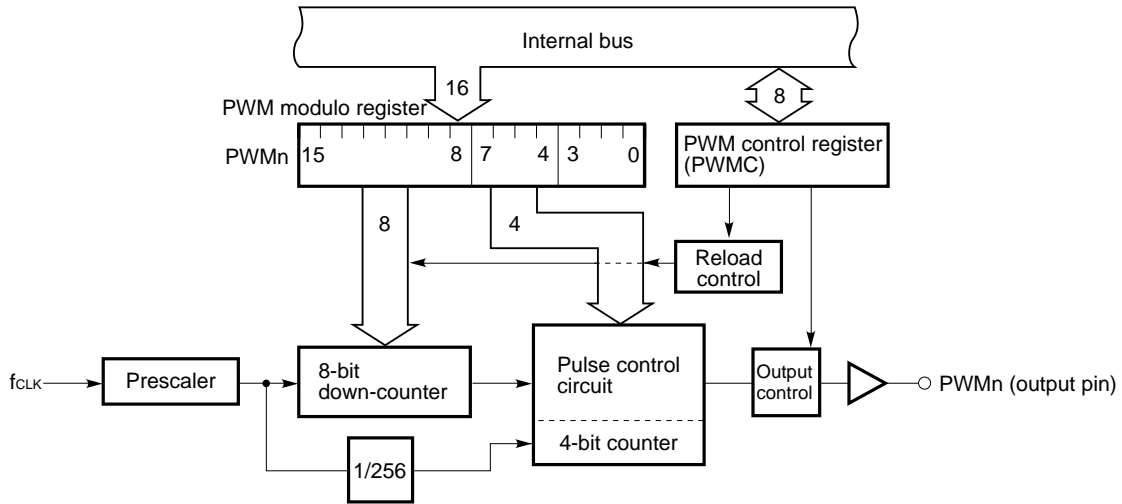


Remark OVF: Overflow flag

8.5 PWM Output (PWM0, PWM1)

Two channels of PWM (pulse width modulation) output circuitry with a resolution of 12 bits and a repetition frequency of 62.5 kHz ($f_{CLK} = 16 \text{ MHz}$) are incorporated. Low or high active level can be selected for the PWM output channels, independently of each other. This output is best suited to DC motor speed control.

Figure 8-6. Block Diagram of PWM Output Unit



Remark n = 0, 1

8.6 A/D Converter

An analog/digital (A/D) converter having 8 multiplexed analog inputs (ANI0-ANI7) is incorporated.

The successive approximation system is used for conversion. The result of conversion is held in the 8-bit A/D conversion result register (ADCR). Thus, speedy high-precision conversion can be achieved. (The conversion time is about 7.5 μs at f_{CLK} = 16 MHz.)

A/D conversion can be started in any of the following modes:

- Hardware start: Conversion is started by means of trigger input (INTP5).
- Software start : Conversion is started by means of bit setting the A/D converter mode register (ADM).

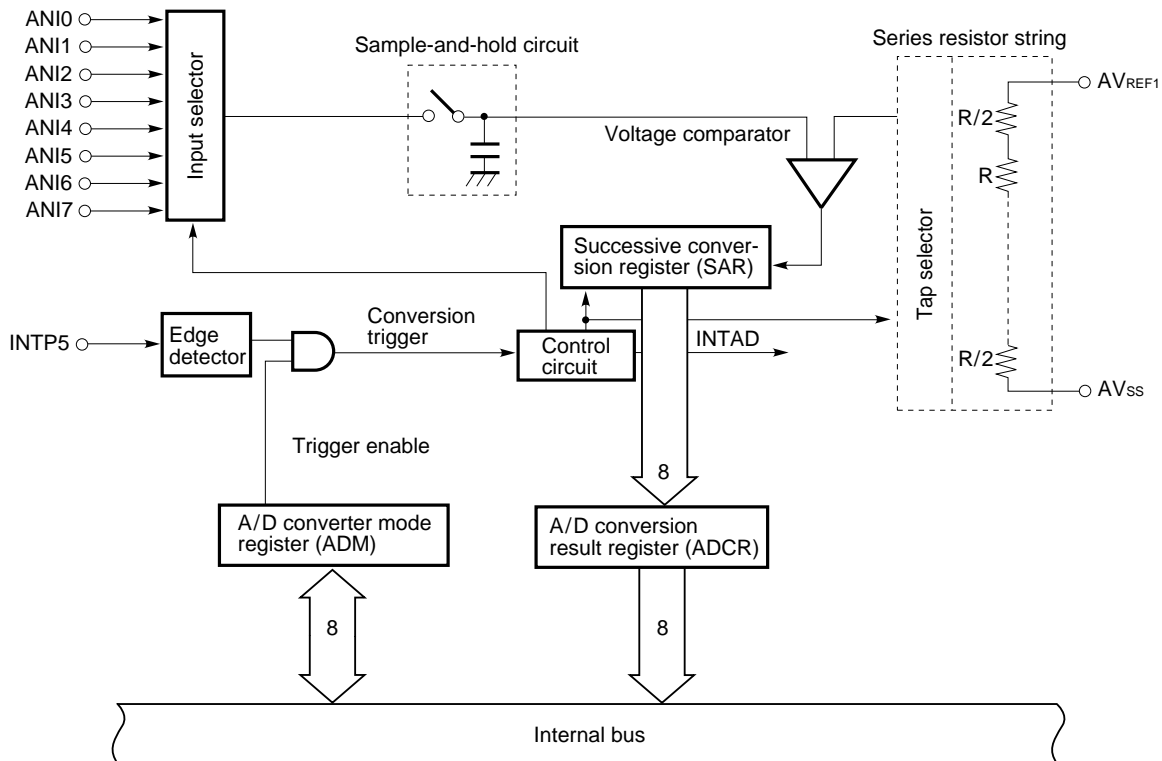
After conversion has started, one of the following modes can be selected:

- Scan mode : Multiple analog inputs are selected sequentially to obtain conversion data from all pins.
- Select mode: A single analog input is selected at all times to enable conversion data to be obtained continuously.

ADM is used to specify the above modes, as well as the termination of conversion.

When the result of conversion is transferred to ADCR, an interrupt request (INTAD) is generated. Using this feature, the results of conversion can be continuously transferred to memory by the macro service.

Figure 8-7. Block Diagram of A/D Converter



8.7 D/A Converter

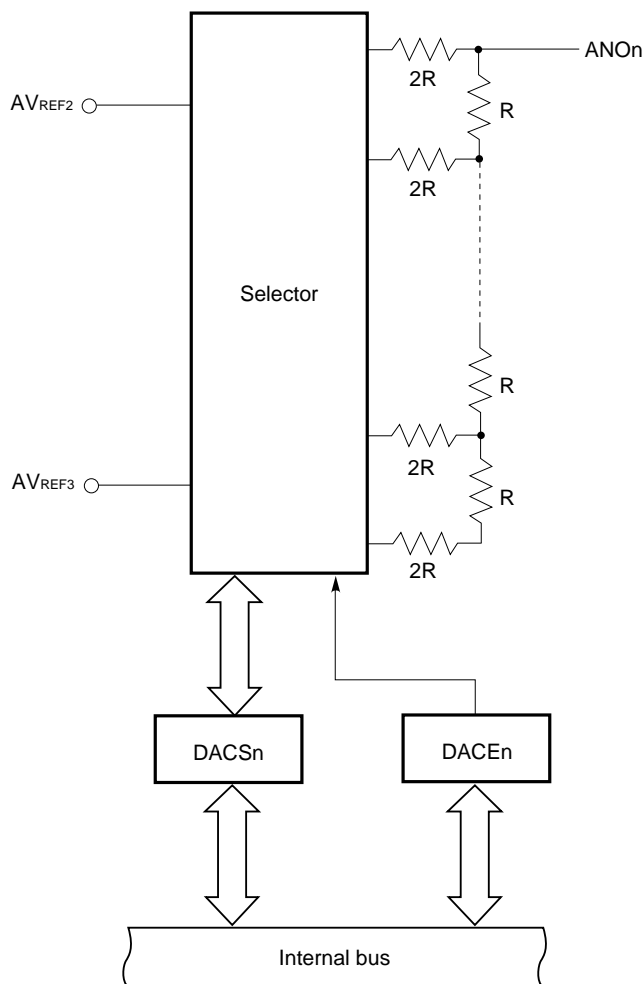
Two digital/analog (D/A) converter channels of voltage output type, having a resolution of 8 bits, are incorporated.

An R-2R resistor ladder system is used for conversion. By writing the value to be subject to D/A conversion in the 8-bit D/A conversion value setting register (DACSn: n = 0, 1), the resulting analog value is output on ANOn (n = 0, 1). The range of the output voltages is determined by the voltages applied to the AVREF2 and AVREF3 pins.

Because of its high output impedance, no current can be obtained from an output pin. When the load impedance is low, insert a buffer amplifier between the load and the converter.

The impedance of the ANOn pin goes high while the RESET signal is low. DACSn is set to 0 after a reset is released.

Figure 8-8. Block Diagram of D/A Converter



Remark n = 0, 1

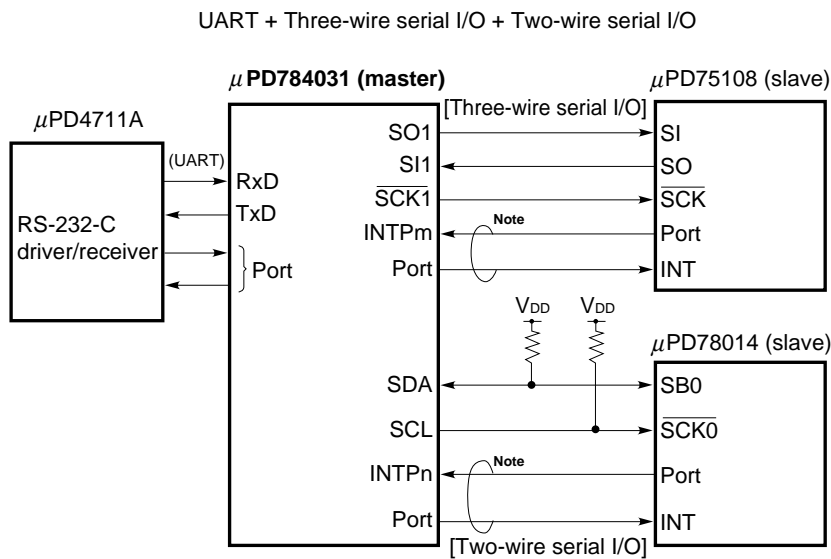
8.8 Serial Interface

Three independent serial interface channels are incorporated.

- Asynchronous serial interface (UART)/three-wire serial I/O (IOE) × 2
- Synchronous serial interface (CSI) × 1
 - Three-wire serial I/O (IOE)
 - Two-wire serial I/O (IOE)

So, communication with points external to the system and local communication within the system can be performed at the same time. (See **Figure 8-9.**)

Figure 8-9. Example Serial Interfaces



Note Handshake line

8.8.1 Asynchronous serial interface/three-wire serial I/O (UART/IOE)

Two serial interface channels are available; for each channel, asynchronous serial interface mode or three-wire serial I/O mode can be selected.

(1) Asynchronous serial interface mode

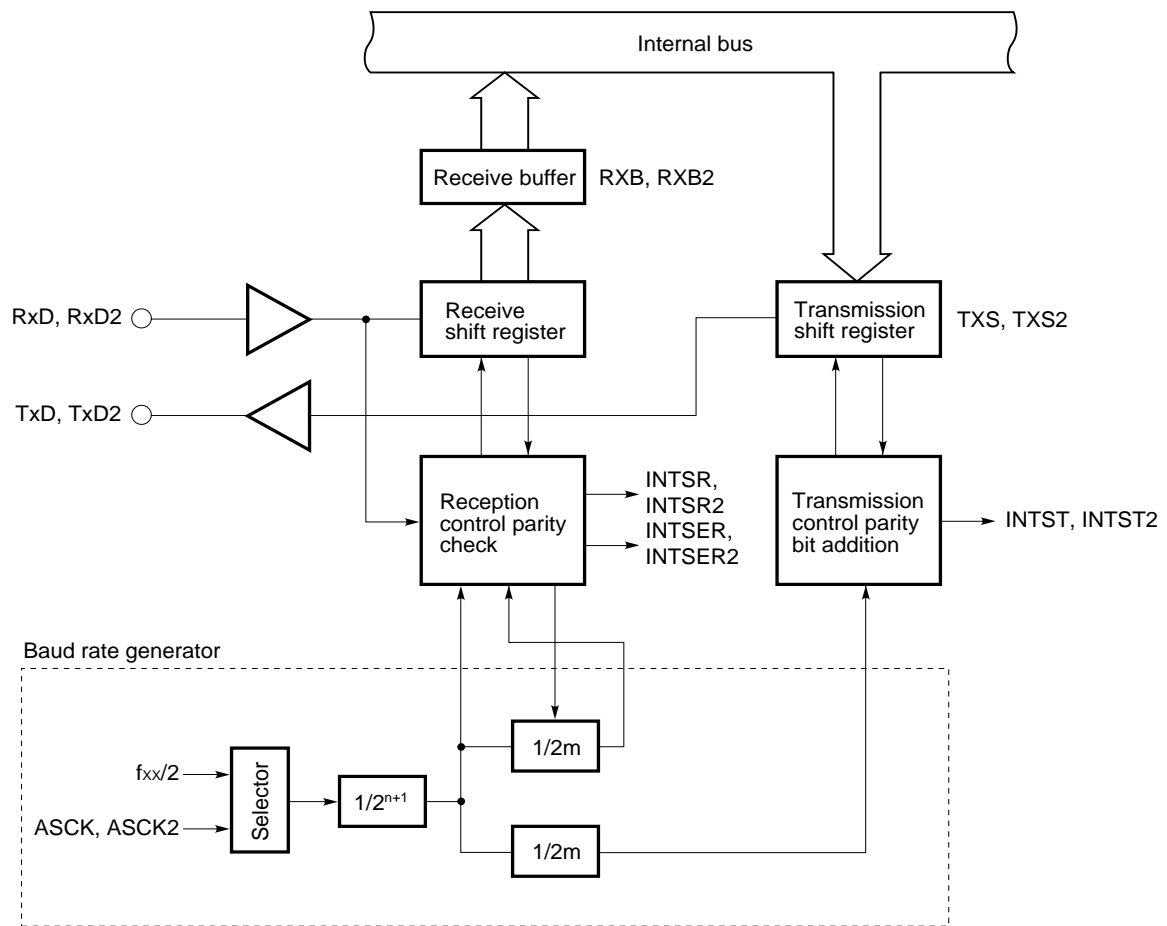
In this mode, 1-byte data is transferred after a start bit.

A baud rate generator is incorporated to enable communication at a wide range of baud rates.

Moreover, the frequency of a clock signal applied to the ASCK pin can be divided to define a baud rate.

With the baud rate generator, the baud rate conforming to the MIDI standard (31.25 kbps) can be obtained.

Figure 8-10. Block Diagram of Asynchronous Serial Interface Mode



Remark f_{xx} : Oscillator frequency or external clock input
 $n = 0$ to 11
 $m = 16$ to 30

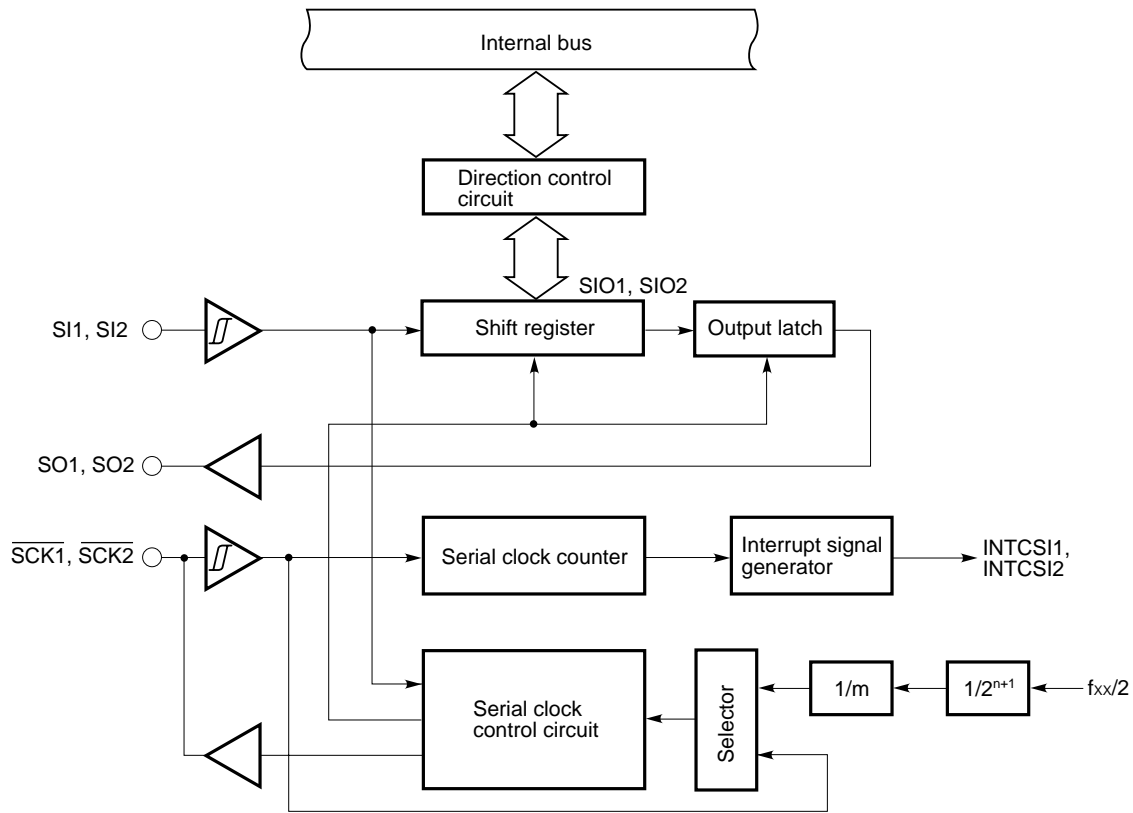
(2) Three-wire serial I/O mode

In this mode, the master device makes the serial clock active to start transmission, then transfers 1-byte data in phase with the clock.

This mode is designed for communication with a device incorporating a conventional synchronous serial interface. Basically, three lines are used for communication: the serial clock line (\overline{SCK}) and the two serial data lines (SI and SO).

In general, a handshake line is required to check the state of communication.

Figure 8-11. Block Diagram of Three-Wire Serial I/O Mode



Remark f_{xx} : Oscillator frequency or external clock input

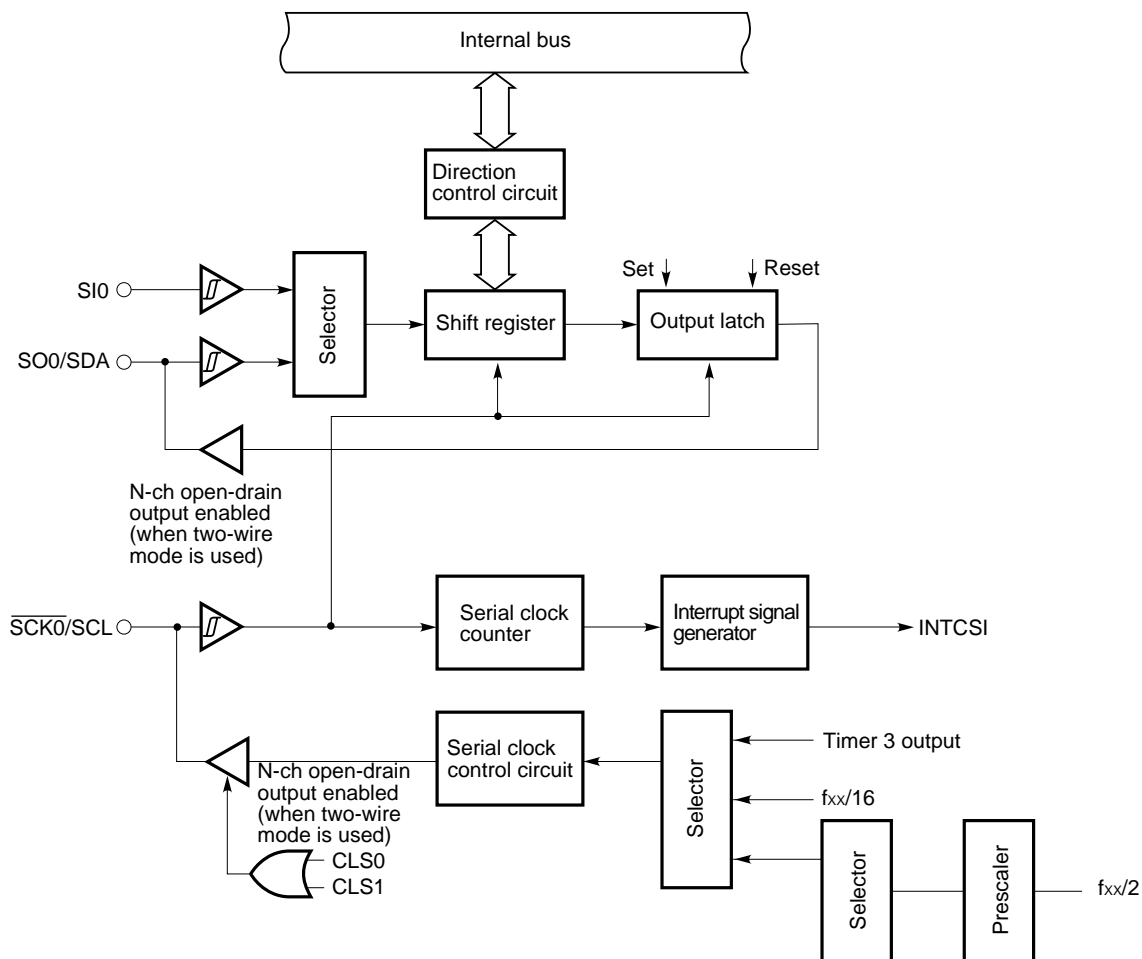
$n = 0$ to 11

$m = 1, 16$ to 30

8.8.2 Synchronous serial interface (CSI)

With this interface, the master device makes the serial clock active to start transmission, then transfers 1-byte data in phase with the clock.

Figure 8-12. Block Diagram of Synchronous Serial Interface



Remark f_{xx}: Oscillator frequency or external clock input

(1) Three-wire serial I/O mode

This mode is designed for communication with a device incorporating a conventional synchronous serial interface. Basically, three lines are used for communication: the serial clock line ($\overline{SCK0}$) and serial data lines (SI0 and SO0). In general, a handshake line is required to check the state of communication.

(2) Two-wire serial I/O mode

In this mode, 8-bit data is transferred using two lines: the serial clock line (SCL) and serial data bus (SDA). In general, a handshake line is required to check the communication state.

8.9 Edge Detection Function

The interrupt input pins (NMI, INTP0-INTP5) are used to apply not only interrupt requests but also trigger signals for the built-in circuits. As these pins are triggered by an edge (rising or falling) of an input signal, a function for edge detection is incorporated. Moreover, a noise suppression function is provided to prevent erroneous edge detection caused by noise.

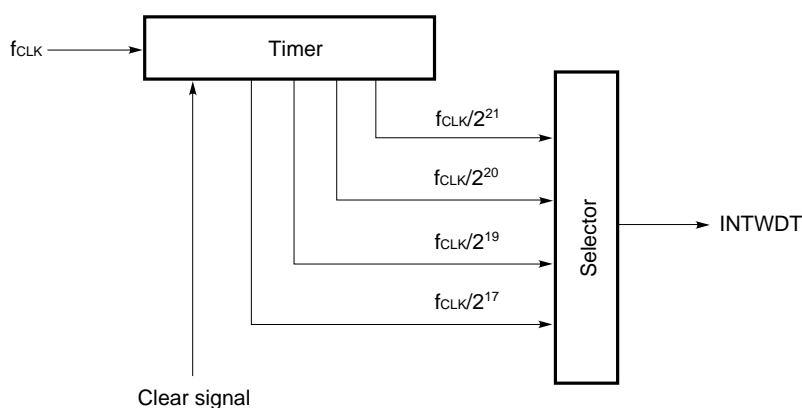
| Pin | Detectable edge | Noise suppression method |
|--------------|--|--------------------------------|
| NMI | Rising edge or falling edge | Analog delay |
| INTP0-INTP3 | Rising edge or falling edge, or both edges | Clock sampling ^{Note} |
| INTP4, INTP5 | | Analog delay |

Note INTP0 is used for sampling clock selection.

8.10 Watchdog Timer

A watchdog timer is incorporated for CPU runaway detection. The watchdog timer, if not cleared by software within a specified interval, generates a nonmaskable interrupt. Furthermore, once watchdog timer operation is enabled, it cannot be disabled by software. The user can specify whether priority is placed on an interrupt based on the watchdog timer or on an interrupt based on the NMI pin.

Figure 8-13. Block Diagram of Watchdog Timer



9. INTERRUPT FUNCTION

Table 9-1 lists the interrupt request handling modes. These modes are selected by software.

Table 9-1. Interrupt Request Handling Modes

| Handling mode | Handled by | Handling | PC and PSW contents |
|--------------------|------------|---|---|
| Vectored interrupt | Software | Branches to a handling routine for execution (arbitrary handling). | The PC and PSW contents are pushed to and popped from the stack. |
| Context switching | | Automatically selects a register bank, and branches to a handling routine for execution (arbitrary handling). | The PC and PSW contents are saved to and read from a fixed area in the register bank. |
| Macro service | Firmware | Performs operations such as memory-to-I/O-device data transfer (fixed handling). | Maintained |

9.1 Interrupt Source

★ An interrupt can be issued from any one of the interrupt sources listed in Table 9-2: execution of BRK and BRKCS instructions, an operand error, or any of the 23 other interrupt sources.

Four levels of interrupt handling priority can be set. Priority levels can be set to nest control during interrupt handling or to concurrently generate interrupt requests. Nested macro services, however, are performed without suspension.

When interrupt requests having the same priority level are generated, they are handled according to the default priority (fixed). (See **Table 9-2**.)

★ **Table 9-2. Interrupt Sources**

| Type | Default priority | Source | | Internal/external | Macro service | | |
|-------------|------------------|---|--|-------------------|---------------|----------|---------|
| | | Name | Trigger | | | | |
| Software | - | BRK instruction | Instruction execution | - | - | | |
| | | BRKCS instruction | | | | | |
| | | Operand error | When the MOV STBC,#byte, MOV WDM,#byte, or LOCATION instruction is executed, exclusive OR of the byte operand and byte does not produce FFH. | | | | |
| Nonmaskable | - | NMI | Detection of edge input on the pin | External | - | | |
| | | WDT | Watchdog timer overflow | Internal | | | |
| Maskable | 0 (highest) | INTP0 | Detection of edge input on the pin (TM1/TM1W capture trigger, TM1/TM1W event counter input) | External | Enabled | | |
| | 1 | INTP1 | Detection of edge input on the pin (TM2/TM2W capture trigger, TM2/TM2W event counter input) | | | | |
| | 2 | INTP2 | Detection of edge input on the pin (TM2/TM2W capture trigger, TM2/TM2W event counter input) | | | | |
| | 3 | INTP3 | Detection of edge input on the pin (TM0 capture trigger, TM0 event counter input) | | | | |
| | 4 | INTC00 | TM0-CR00 match signal issued | | | Internal | Enabled |
| | 5 | INTC01 | TM0-CR01 match signal issued | | | | |
| | 6 | INTC10 | TM1-CR10 match signal issued (in 8-bit operation mode) TM1W-CR10W match signal issued (in 16-bit operation mode) | | | | |
| | 7 | INTC11 | TM1-CR11 match signal issued (in 8-bit operation mode) TM1W-CR11W match signal issued (in 16-bit operation mode) | | | | |
| | 8 | INTC20 | TM2-CR20 match signal issued (in 8-bit operation mode) TM2W-CR20W match signal issued (in 16-bit operation mode) | | | | |
| | 9 | INTC21 | TM2-CR21 match signal issued (in 8-bit operation mode) TM2W-CR21W match signal issued (in 16-bit operation mode) | | | | |
| | 10 | INTC30 | TM3-CR30 match signal issued (in 8-bit operation mode) TM3W-CR30W match signal issued (in 16-bit operation mode) | | | | |
| | 11 | INTP4 | Detection of edge input on the pin | External | Enabled | | |
| | 12 | INTP5 | Detection of edge input on the pin | | | | |
| | 13 | INTAD | A/D converter processing completed (ADCR transfer) | Internal | Enabled | | |
| | 14 | INTSER | ASI0 reception error | | - | | |
| | 15 | INTSR | ASI0 reception completed or CSI1 transfer completed | | Enabled | | |
| | | INTCSI1 | | | | | |
| | 16 | INTST | ASI0 transmission completed | | Enabled | | |
| | 17 | INTCSI | CSI0 transfer completed | | | | |
| | 18 | INTSER2 | ASI2 reception error | | - | | |
| 19 | INTSR2 | ASI2 reception completed or CSI2 transfer completed | Enabled | | | | |
| | INTCSI2 | | | | | | |
| 20 (lowest) | INTST2 | ASI2 transmission completed | | | | | |

Remark ASI: Asynchronous serial interface
CSI: Synchronous serial interface

9.2 Vectored Interrupt

When a branch to an interrupt handling routine occurs, the vector table address corresponding to the interrupt source is used as the branch address.

Interrupt handling by the CPU consists of the following operations:

- When a branch occurs : Push the CPU status (PC and PSW contents) to the stack.
- When control is returned: Pop the CPU status (PC and PSW contents) from the stack.

To return control from the handling routine to the main routine, use the RETI instruction. The branch destination addresses must be within the range of 0 to FFFFH.

Table 9-3. Vector Table Address

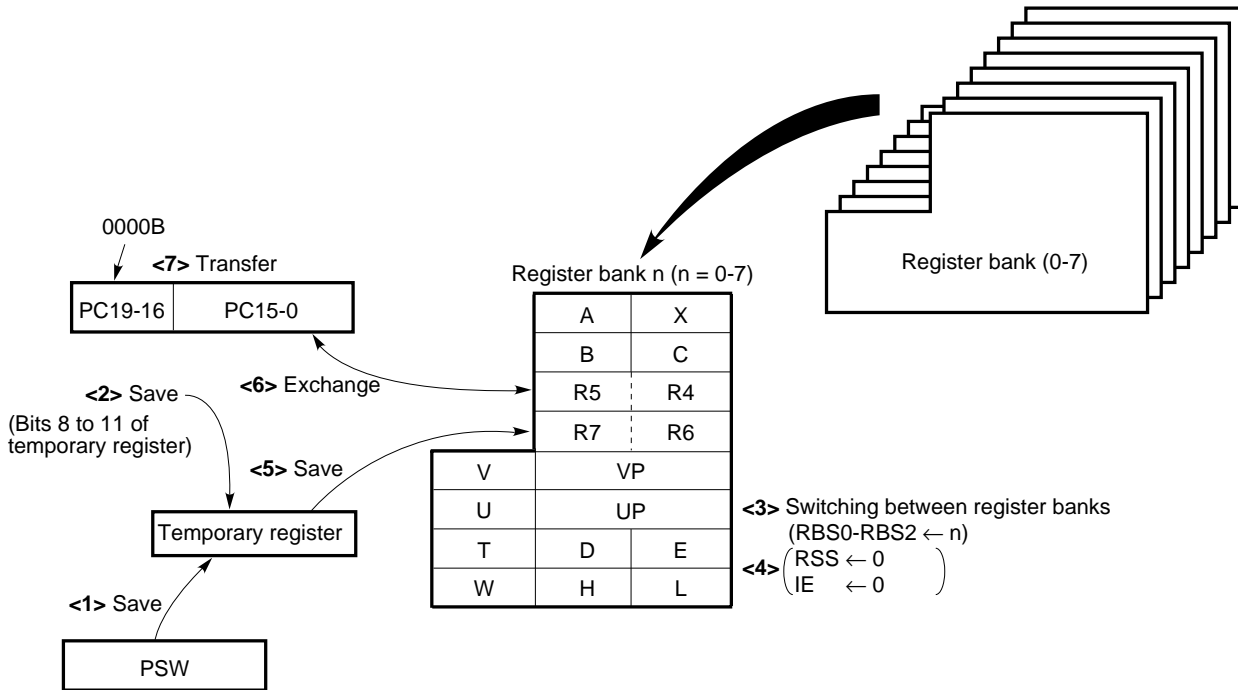
| Interrupt source | Vector table address |
|------------------|----------------------|
| BRK instruction | 003EH |
| Operand error | 003CH |
| NMI | 0002H |
| WDT | 0004H |
| INTP0 | 0006H |
| INTP1 | 0008H |
| INTP2 | 000AH |
| INTP3 | 000CH |
| INTC00 | 000EH |
| INTC01 | 0010H |
| INTC10 | 0012H |
| INTC11 | 0014H |
| INTC20 | 0016H |
| INTC21 | 0018H |
| INTC30 | 001AH |
| INTP4 | 001CH |
| INTP5 | 001EH |
| INTAD | 0020H |
| INTSER | 0022H |
| INTSR | 0024H |
| INTCSI1 | |
| INTST | 0026H |
| INTCSI | 0028H |
| INTSER2 | 002AH |
| INTSR2 | 002CH |
| INTCSI2 | |
| INTST2 | 002EH |

9.3 Context Switching

When an interrupt request is generated, or when the BRKCS instruction is executed, an appropriate register bank is selected by the hardware. Then, a branch to a vector address stored in that register bank occurs. At the same time, the contents of the current program counter (PC) and program status word (PSW) are stacked in the register bank.

The branch address must be within the range of 0 to FFFFH.

Figure 9-1. Context Switching Caused by an Interrupt Request

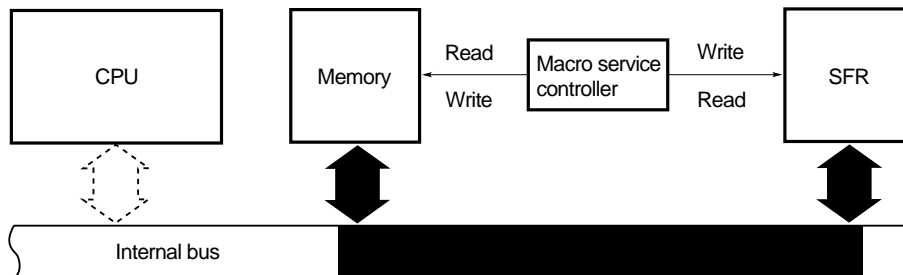


9.4 Macro Service

The macro service function enables data transfer between memory and special function registers (SFRs) without requiring the intervention of the CPU. The macro service controller accesses both memory and SFRs within the same transfer cycle to directly transfer data without having to perform data fetch.

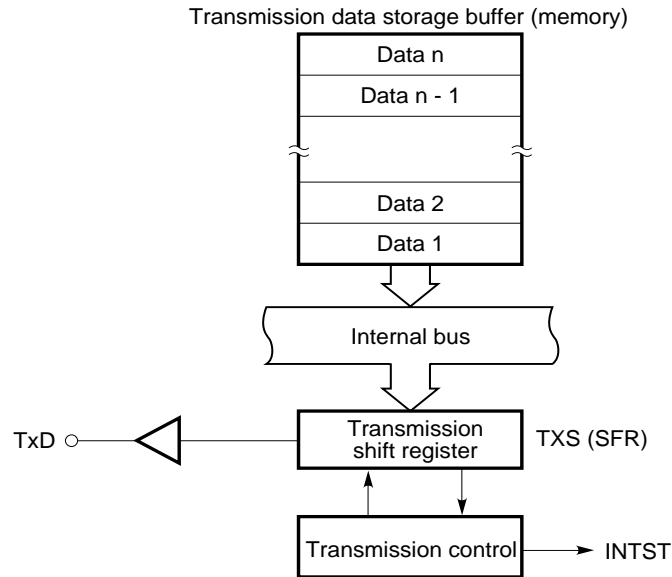
Since the CPU status is neither saved nor restored, nor is data fetch performed, high-speed data transfer is possible.

Figure 9-2. Macro Service



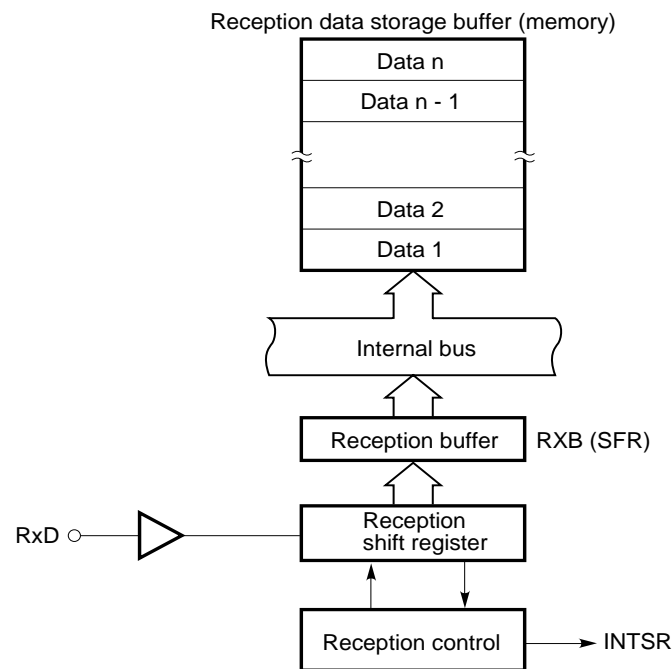
9.5 Examples of Macro Service Applications

(1) Serial interface transmission



Each time a macro service request (INTST) is generated, the next transmission data is transferred from memory to TXS. When data n (last byte) has been transferred to TXS (that is, once the transmission data storage buffer becomes empty), a vectored interrupt request (INTST) is generated.

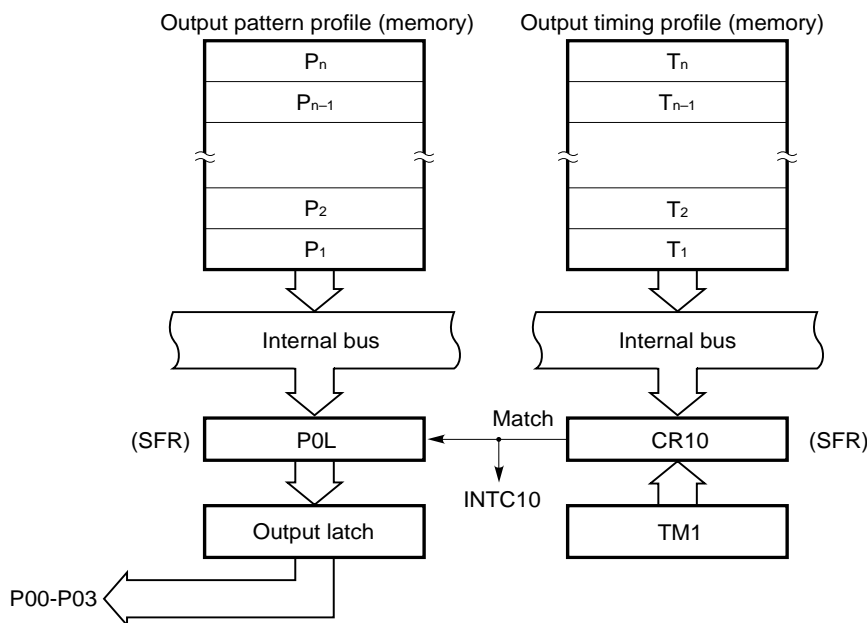
(2) Serial interface reception



Each time a macro service request (INTSR) is generated, reception data is transferred from RXB to memory. When data n (last byte) has been transferred to memory (that is, once the reception data storage buffer becomes full), a vectored interrupt request (INTSR) is generated.

(3) Real-time output port

INTC10 and INTC11 function as the output triggers for the real-time output ports. For these triggers, the macro service can simultaneously set the next output pattern and interval. Therefore, INTC10 and INTC11 can be used to independently control two stepping motors. They can also be applied to PWM and DC motor control.

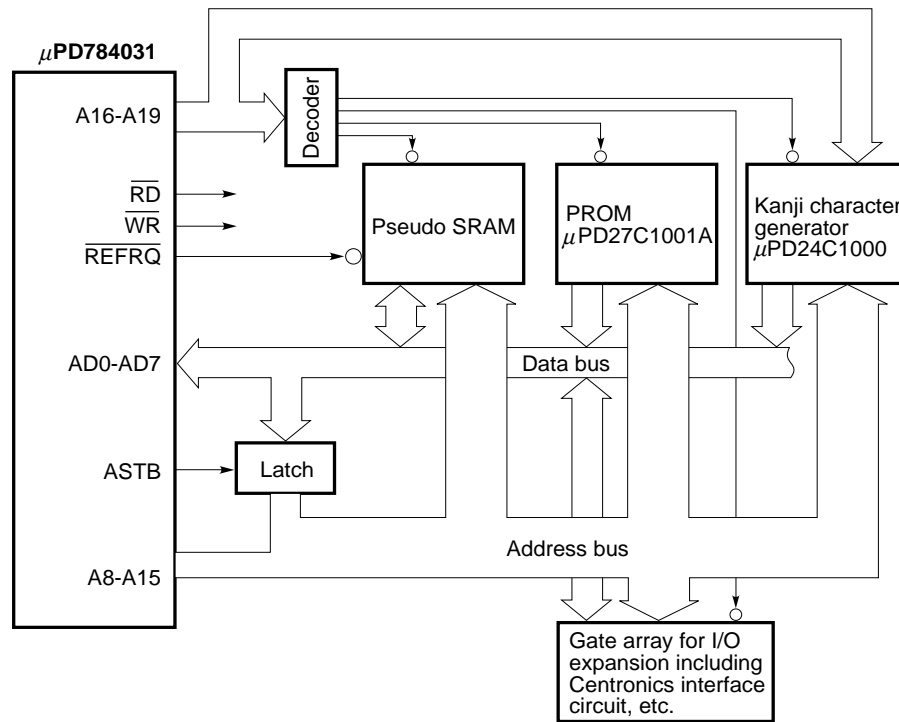


Each time a macro service request (INTC10) is generated, a pattern and timing data are transferred to the buffer register (P0L) and compare register (CR10), respectively. When the contents of timer register 1 (TM1) and CR10 match, another INTC10 is generated, and the P0L contents are transferred to the output latch. When Tn (last byte) is transferred to CR10, a vectored interrupt request (INTC10) is generated. For INTC11, the same operation as that performed for INTC10 is performed.

10. LOCAL BUS INTERFACE

The local bus interface enables the connection of external memory and I/O devices (memory-mapped I/O). It supports a 1M-byte memory space. (See Figure 10-1.)

Figure 10-1. Example of Local Bus Interface



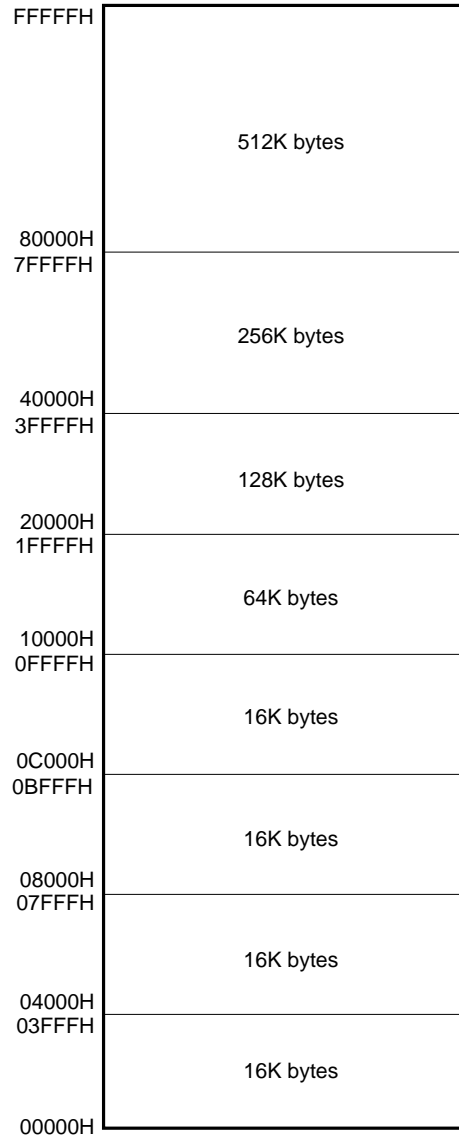
10.1 Memory Expansion

By adding external memory, program memory or data memory can be expanded, 256 bytes at a time, to approximately 1M byte (seven steps).

10.2 Memory Space

The 1M-byte memory space is divided into eight spaces, each having a logical address. Each of these spaces can be controlled using the programmable wait and pseudo-static RAM refresh functions.

Figure 10-2. Memory Space



10.3 Programmable Wait

When the memory space is divided into eight spaces, a wait state can be separately inserted for each memory space while the \overline{RD} or \overline{WR} signal is active. This prevents the overall system efficiency from being degraded even when memory devices having different access times are connected.

In addition, an address wait function that extends the ASTB signal active period is provided to produce a longer address decode time. (This function is set for the entire space.)

10.4 Pseudo-Static RAM Refresh Function

Refresh is performed as follows:

- Pulse refresh : A bus cycle is inserted where a refresh pulse is output on the \overline{REFRQ} pin at regular intervals. When the memory space is divided into eight, and a specified area is being accessed, refresh pulses can also be output on the \overline{REFRQ} pin as the memory is being accessed. This can prevent the refresh cycle from suspending normal memory access.
- Power-down self-refresh : In standby mode, a low-level signal is output on the \overline{REFRQ} pin to maintain the contents of pseudo-static RAM.

10.5 Bus Hold Function

A bus hold function is provided to facilitate connection to devices such as a DMA controller. Suppose that a bus hold request signal (HLDRQ) is received from an external bus master. In this case, upon the completion of the bus cycle being performed, the address bus, address/data bus, ASTB, \overline{RD} , and \overline{WR} pins are placed in the high-impedance state, and the bus hold acknowledge signal (HLDAK) is made active to release the bus for the external bus master.

While the bus hold function is being used, the external wait and pseudo-static RAM refresh functions are disabled.

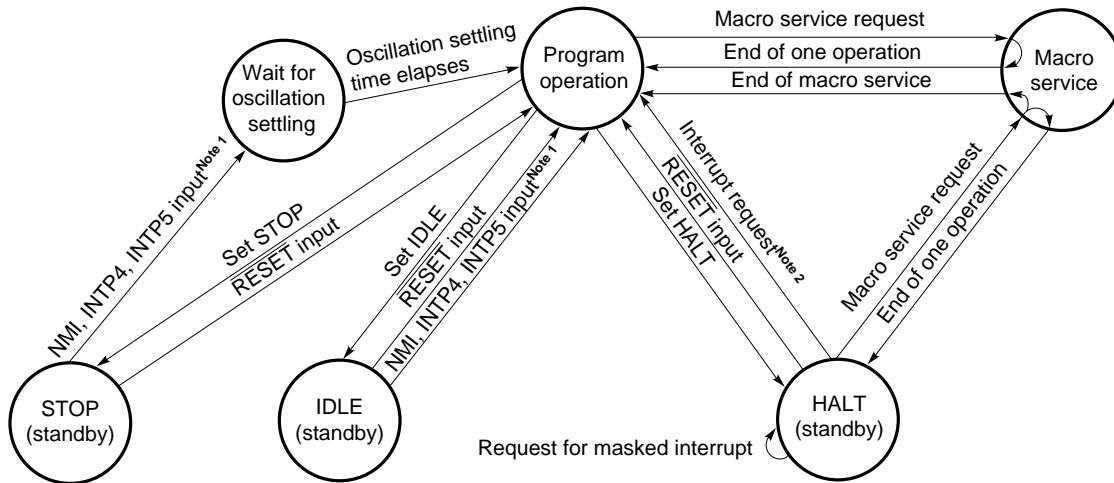
11. STANDBY FUNCTION

The standby function allows the power consumption of the chip to be reduced. The following standby modes are supported:

- HALT mode : The CPU operation clock is stopped. By occasionally inserting the HALT mode during normal operation, the overall average power consumption can be reduced.
- IDLE mode : The entire system is stopped, with the exception of the oscillator circuit. This mode consumes only very little more power than STOP mode, but normal program operation can be restored in almost as little time as that required to restore normal program operation from HALT mode.
- STOP mode : The oscillator is stopped. All operations in the chip stop, such that only leakage current flows.

These modes can be selected by software.
A macro service can be initiated in HALT mode.

Figure 11-1. Standby Mode Status Transition



- Notes**
1. INTP4 and INTP5 are applied when not masked.
 2. Only when the interrupt request is not masked

Remark NMI is enabled only by external input. The watchdog timer cannot be used to release one of the standby modes (STOP or IDLE mode).

12. RESET FUNCTION

Applying a low-level signal to the $\overline{\text{RESET}}$ pin initializes the internal hardware (reset status).

When the $\overline{\text{RESET}}$ input makes a low-to-high transition, the following data is loaded into the program counter (PC):

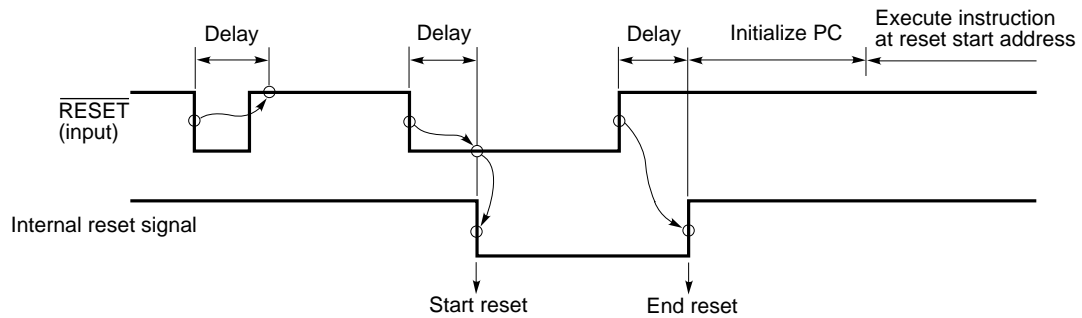
- Eight low-order bits of the PC : Contents of location at address 0000H
- Intermediate eight bits of the PC : Contents of location at address 0001H
- Four high-order bits of the PC : 0

The PC contents are used as a branch destination address. Program execution starts from that address. Therefore, a reset start can be performed from an arbitrary address.

The contents of each register can be set by software, as required.

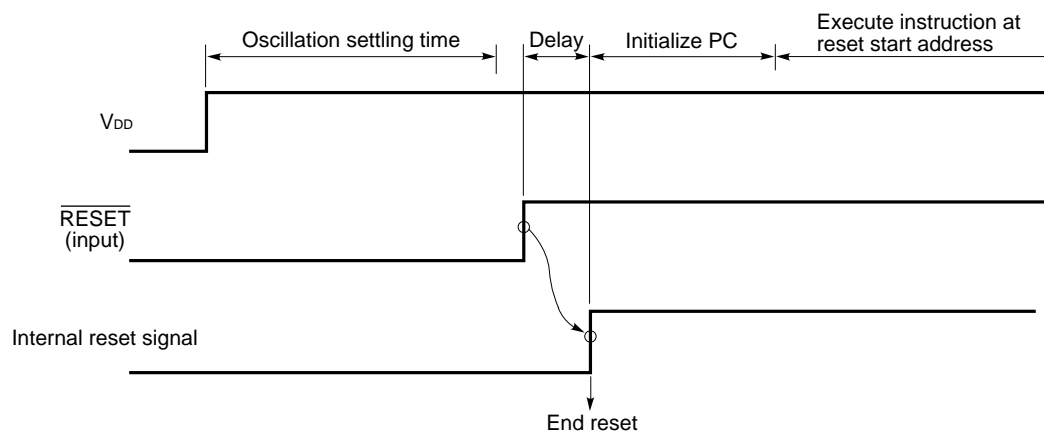
The $\overline{\text{RESET}}$ input circuit contains a noise eliminator to prevent malfunctions caused by noise. This noise eliminator is an analog delay sampling circuit.

Figure 12-1. Accepting a Reset



For power-on reset, the $\overline{\text{RESET}}$ signal must be held active until the oscillation settling time (approximately 40 ms) has elapsed.

Figure 12-2. Power-On Reset



13. INSTRUCTION SET

(1) 8-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where A is described as r.)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVW, XCHW, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 13-1. Instructions Implemented by 8-Bit Addressing

| 2nd operand 1st operand | #byte | A | r r' | saddr saddr' | sfr | !addr16 !!addr24 | mem [saddrp] [%saddrg] | r3 PSWL PSWH | [WHL+] [WHL-] | n | NoneNote 2 |
|------------------------------|--------------------|------------------------------------|---------------------------|---|-----------------------------|-----------------------------|------------------------------|--------------------|-------------------------------|-----------|------------------------------|
| A | (MOV) ADDNote 1 | (MOV) (XCH) (ADD)Note 1 | MOV XCH (ADD)Note 1 | (MOV)Note 6 (XCH)Note 6 (ADD)Notes 1, 6 | MOV (XCH) (ADD)Note 1 | (MOV) (XCH) ADDNote 1 | MOV XCH ADDNote 1 | MOV | (MOV) (XCH) (ADD)Note 1 | | |
| r | MOV ADDNote 1 | (MOV) (XCH) (ADD)Note 1 | MOV XCH ADDNote 1 | MOV XCH ADDNote 1 | MOV XCH ADDNote 1 | MOV XCH | | | | RORNote 3 | MULU DIVUW INC DEC |
| saddr | MOV ADDNote 1 | (MOV)Note 6 (ADD)Note 1 | MOV ADDNote 1 | MOV XCH ADDNote 1 | | | | | | | INC DEC DBNZ |
| sfr | MOV ADDNote 1 | MOV (ADD)Note 1 | MOV ADDNote 1 | | | | | | | | PUSH POP CHKL CHKLA |
| !addr16 !!addr24 | MOV | (MOV) ADDNote 1 | MOV | | | | | | | | |
| mem [saddrp] [%saddrg] | | MOV ADDNote 1 | | | | | | | | | |
| mem3 | | | | | | | | | | | ROR4 ROL4 |
| r3 PSWL PSWH | MOV | MOV | | | | | | | | | |
| B, C | | | | | | | | | | | DBNZ |
| STBC, WDM | MOV | | | | | | | | | | |
| [TDE+] [TDE-] | | (MOV) (ADD)Note 1 MOVWNote 4 | | | | | | | MOVBKNote 5 | | |

- Notes**
1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.
 2. There is no second operand, or the second operand is not an operand address.
 3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.
 4. XCHW, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVW.
 5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.
 6. When saddr is saddr2 with this combination, an instruction with a short code exists.

(2) 16-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where AX is described as rp.)

MOVW, XCHW, ADDW, SUBW, CMPW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 13-2. Instructions Implemented by 16-Bit Addressing

| 2nd operand 1st operand | #word | AX | rp rp' | saddrp saddrp' | strp | !addr16 !!addr24 | mem [saddrp] [%saddrg] | [WHL+] | byte | n | None ^{Note 2} |
|------------------------------|----------------------------------|--|--|---|--|---------------------|------------------------------|------------------|---------|--------------|--|
| AX | (MOVW) ADDW ^{Note 1} | (MOVW) (XCHW) (ADD) ^{Note 1} | (MOVW) (XCHW) (ADDW) ^{Note 1} | (MOVW) ^{Note 3} (XCHW) ^{Note 3} (ADDW) ^{Notes 1,3} | MOVW (XCHW) (ADDW) ^{Note 1} | (MOVW) XCHW | MOVW XCHW | (MOVW) (XCHW) | | | |
| rp | MOVW ADDW ^{Note 1} | (MOVW) (XCHW) (ADDW) ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | MOVW | | | | SHRW SHLW | MULW ^{Note 4} INCW DECW |
| saddrp | MOVW ADDW ^{Note 1} | (MOVW) ^{Note 3} (ADDW) ^{Note 1} | MOVW ADDW ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | | | | | | | INCW DECW |
| sfrp | MOVW ADDW ^{Note 1} | MOVW (ADDW) ^{Note 1} | MOVW ADDW ^{Note 1} | | | | | | | | PUSH POP |
| !addr16 !!addr24 | MOVW | (MOVW) | MOVW | | | | | | MOVTBLW | | |
| mem [saddrp] [%saddrg] | | MOVW | | | | | | | | | |
| PSW | | | | | | | | | | | PUSH POP |
| SP | ADDWG SUBWG | | | | | | | | | | |
| post | | | | | | | | | | | PUSH POP PUSHU POPU |
| [TDE+] | | (MOVW) | | | | | | SACW | | | |
| byte | | | | | | | | | | | MACW MACSW |

- Notes**
1. SUBW and CMPW are the same as ADDW.
 2. There is no second operand, or the second operand is not an operand address.
 3. When saddrp is saddrp2 with this combination, an instruction with a short code exists.
 4. MULW and DIVUX are the same as MULW.

(3) 24-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where WHL is described as rg.)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 13-3. Instructions Implemented by 24-Bit Addressing

| 2nd operand 1st operand | #imm24 | WHL | rg rg' | saddrg | !!addr24 | mem1 | [%saddrg] | SP | NoneNote |
|----------------------------|----------------------------|----------------------------|----------------------------|------------------------|----------|------|-----------|------|-----------------------------|
| WHL | (MOVG) (ADDG) (SUBG) | (MOVG) (ADDG) (SUBG) | (MOVG) (ADDG) (SUBG) | (MOVG) ADDG SUBG | (MOVG) | MOVG | MOVG | MOVG | |
| rg | MOVG ADDG SUBG | (MOVG) (ADDG) (SUBG) | MOVG ADDG SUBG | MOVG | MOVG | | | | INCG DECG PUSH POP |
| saddrg | | (MOVG) | MOVG | | | | | | |
| !!addr24 | | (MOVG) | MOVG | | | | | | |
| mem1 | | MOVG | | | | | | | |
| [%saddrg] | | MOVG | | | | | | | |
| SP | MOVG | MOVG | | | | | | | INCG DECG |

Note There is no second operand, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 13-4. Bit Manipulation Instructions Implemented by Addressing

| | | | | |
|---|------|---|--|-----------------------------|
| 2nd operand / | CY | saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit | /saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit | None <small>Note</small> |
| 1st operand | | | | |
| CY | | MOV1 AND1 OR1 XOR1 | AND1 OR1 | NOT1 SET1 CLR1 |
| saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit | MOV1 | | SET1 CLR1 BF BT BTCLR BFSET | NOT1 |

Note There is no second operand, or the second operand is not an operand address.

(5) Call/return instructions and branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 13-5. Call/Return and Branch Instructions Implemented by Addressing

| Instruction address operand | \$addr20 | !addr20 | !addr16 | !!addr20 | rp | rg | [rp] | [rg] | !addr11 | [addr5] | RBn | None |
|-----------------------------|------------------------------------|------------|-------------------------------|------------|------------|------------|------------|------------|---------|---------|-------|----------------------------|
| Basic instruction | BC ^{Note} BR | CALL BR | CALL BR RETCS RETCSB | CALL BR | CALL BR | CALL BR | CALL BR | CALL BR | CALLF | CALLF | BRKCS | BRK RET RETI RETB |
| Composite instruction | BF BT BTCLR BFSET DBNZ | | | | | | | | | | | |

Note BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJSB, CVTBW, LOCATION, SEL, NOT EI, DI, SWRS

★ 14. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

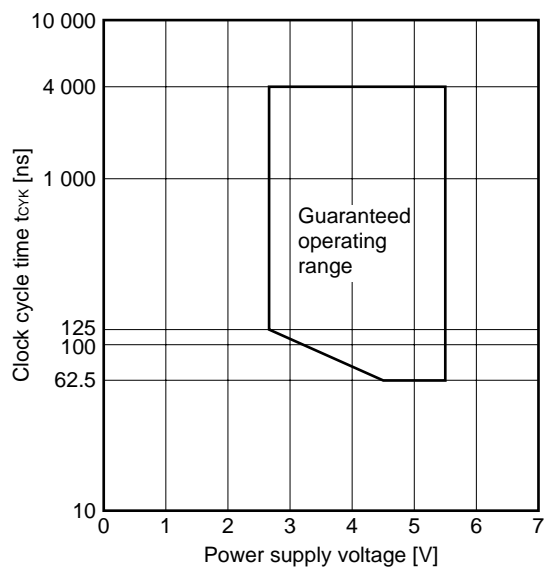
| Parameter | Symbol | Conditions | Rating | Unit |
|---------------------------------------|--------------------|--------------------------|---|------|
| Supply voltage | V _{DD} | | -0.5 to +7.0 | V |
| | AV _{DD} | | AV _{SS} to V _{DD} + 0.5 | V |
| | AV _{SS} | | -0.5 to +0.5 | V |
| Input voltage | V _I | | -0.5 to V _{DD} + 0.5 | V |
| Output voltage | V _O | | -0.5 to V _{DD} + 0.5 | V |
| Output low current | I _{OL} | At one pin | 15 | mA |
| | | Total of all output pins | 100 | mA |
| Output high current | I _{OH} | At one pin | -10 | mA |
| | | Total of all output pins | -100 | mA |
| A/D converter reference input voltage | AV _{REF1} | | -0.5 to V _{DD} + 0.3 | V |
| D/A converter reference input voltage | AV _{REF2} | | -0.5 to V _{DD} + 0.3 | V |
| | AV _{REF3} | | -0.5 to V _{DD} + 0.3 | V |
| Operating ambient temperature | T _A | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | -65 to +150 | °C |

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

OPERATING CONDITIONS

- Operating ambient temperature (T_A) : -40 to +85 °C
- Rise time and fall time (t_r, t_f) (at pins which are not specified) : 0 to 200 μs
- Power supply voltage and clock cycle time : See **Figure 14-1**.

Figure 14-1. Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------|-----------------|--------------------------------------|------|------|------|------|
| Input capacitance | C _i | f = 1 MHz | | | 10 | pF |
| Output capacitance | C _o | 0 V on pins other than measured pins | | | 10 | pF |
| I/O capacitance | C _{io} | | | | 10 | pF |

OSCILLATOR CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = +4.5$ to 5.5 V, $V_{SS} = 0$ V)

| Resonator | Recommended circuit | Parameter | MIN. | MAX. | Unit |
|------------------------------|---------------------|--|------|------|------|
| Ceramic resonator or crystal | | Oscillator frequency (f_{xx}) | 4 | 32 | MHz |
| External clock | | X1 input frequency (f_x) | 4 | 32 | MHz |
| | | X1 input rise and fall times (t_{xR} , t_{xF}) | 0 | 10 | ns |
| | | X1 input high-level and low-level widths (t_{WXH} , t_{WXL}) | 10 | 125 | ns |

Caution When using the system clock generator, run wires in the portion surrounded by broken lines according to the following rules to avoid effects such as stray capacitance:

- Minimize the wiring.
- Never cause the wires to cross other signal lines.
- Never cause the wires to run near a line carrying a large varying current.
- Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS1} . Never connect the capacitor to a ground pattern carrying a large current.
- Never extract a signal from the oscillator.

OSCILLATOR CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = +2.7$ to 5.5 V, $V_{SS} = 0$ V)

| Resonator | Recommended circuit | Parameter | MIN. | MAX. | Unit |
|------------------------------|---------------------|--|------|------|------|
| Ceramic resonator or crystal | | Oscillator frequency (f_{xx}) | 4 | 16 | MHz |
| External clock | | X1 input frequency (f_x) | 4 | 16 | MHz |
| | | X1 input rise and fall times (t_{xR} , t_{xF}) | 0 | 10 | ns |
| | | X1 input high-level and low-level widths (t_{wxH} , t_{wxL}) | 10 | 125 | ns |

Caution When using the system clock generator, run wires in the portion surrounded by broken lines according to the following rules to avoid effects such as stray capacitance:

- Minimize the wiring.
- Never cause the wires to cross other signal lines.
- Never cause the wires to run near a line carrying a large varying current.
- Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS1} . Never connect the capacitor to a ground pattern carrying a large current.
- Never extract a signal from the oscillator.

DC CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = AV_{DD} = +2.7$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V) (1/2)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------|-----------|--|----------------|------|----------------|------|
| Input low voltage | V_{IL1} | For pins other than those described in Notes 1, 2, 3, and 4 | -0.3 | | $0.3V_{DD}$ | V |
| | V_{IL2} | For pins described in Notes 1, 2, 3, and 4 | -0.3 | | $0.2V_{DD}$ | V |
| | V_{IL3} | $V_{DD} = +5.0$ V \pm 10 % For pins described in Notes 2, 3, and 4 | -0.3 | | +0.8 | V |
| Input high voltage | V_{IH1} | For pins other than those described in Note 1 | $0.7V_{DD}$ | | $V_{DD} + 0.3$ | V |
| | V_{IH2} | For pins described in Note 1 | $0.8V_{DD}$ | | $V_{DD} + 0.3$ | V |
| | V_{IH3} | $V_{DD} = +5.0$ V \pm 10 % For pins described in Notes 2, 3, and 4 | 2.2 | | $V_{DD} + 0.3$ | V |
| Output low voltage | V_{OL1} | $I_{OL} = 2$ mA | | | 0.4 | V |
| | V_{OL2} | $V_{DD} = +5.0$ V \pm 10 % $I_{OL} = 8$ mA For pins described in Notes 2 and 5 | | | 1.0 | V |
| Output high voltage | V_{OH1} | $I_{OH} = -2$ mA | $V_{DD} - 1.0$ | | | V |
| | V_{OH2} | $V_{DD} = +5.0$ V \pm 10 % $I_{OH} = -5$ mA For pins described in Note 4 | $V_{DD} - 1.4$ | | | V |
| X1 input low current | I_{IL} | EXTC = 0 0 V $\leq V_I \leq V_{IL2}$ | | | -30 | μA |
| X1 input high current | I_{IH} | EXTC = 0 $V_{IH2} \leq V_I \leq V_{DD}$ | | | +30 | μA |

- Notes**
1. X1, X2, $\overline{\text{RESET}}$, P12/ $\overline{\text{ASCK2/SCK2}}$, P20/ $\overline{\text{NMI}}$, P21/ $\overline{\text{INTP0}}$, P22/ $\overline{\text{INTP1}}$, P23/ $\overline{\text{INTP2/CI}}$, P24/ $\overline{\text{INTP3}}$, P25/ $\overline{\text{INTP4/ASCK/SCK1}}$, P26/ $\overline{\text{INTP5}}$, P27/ $\overline{\text{SI0}}$, P32/ $\overline{\text{SCK0/SCL}}$, P33/ $\overline{\text{SO0/SDA}}$, TEST
 2. AD0-AD7, A8-A15
 3. P60/A16-P63/A19, $\overline{\text{RD}}$, $\overline{\text{WR}}$, P66/ $\overline{\text{WAIT/HLDRQ}}$, P67/ $\overline{\text{REFRQ/HLDAK}}$
 4. P00-P07
 5. P10-P17

DC CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = AV_{DD} = +2.7$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V) (2/2)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--------------------------------|-----------|---|--|------|------|------|----|
| Input leakage current | I_{Li} | $0\text{ V} \leq V_i \leq V_{DD}$ For pins other than X1 when EXTC = 0 | | | ±10 | μA | |
| Output leakage current | I_{Lo} | $0\text{ V} \leq V_o \leq V_{DD}$ | | | ±10 | μA | |
| V _{DD} supply current | I_{DD1} | Operation mode | $f_{XX} = 32\text{ MHz}$ $V_{DD} = +5.0\text{ V} \pm 10\%$ | | 25 | 45 | mA |
| | | | $f_{XX} = 16\text{ MHz}$ $V_{DD} = +2.7\text{ to }3.3\text{ V}$ | | 12 | 25 | mA |
| | I_{DD2} | HALT mode | $f_{XX} = 32\text{ MHz}$ $V_{DD} = +5.0\text{ V} \pm 10\%$ | | 13 | 26 | mA |
| | | | $f_{XX} = 16\text{ MHz}$ $V_{DD} = +2.7\text{ to }3.3\text{ V}$ | | 8 | 12 | mA |
| | I_{DD3} | IDLE mode (EXTC = 0) | $f_{XX} = 32\text{ MHz}$ $V_{DD} = +5.0\text{ V} \pm 10\%$ | | | 12 | mA |
| | | | $f_{XX} = 16\text{ MHz}$ $V_{DD} = +2.7\text{ to }3.3\text{ V}$ | | | 8 | mA |
| Pull-up resistor | R_L | $V_i = 0\text{ V}$ | 15 | | 80 | kΩ | |

AC CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = AV_{DD} = +2.7$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V)

(1) Read/write operation (1/2)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|--------|------------------------------|------------------------------|----------------------|------|
| Address setup time | tsAST | $V_{DD} = +5.0$ V \pm 10 % | (0.5 + a) T - 15 | | ns |
| | | | (0.5 + a) T - 31 | | ns |
| ASTB high-level width | twSTH | $V_{DD} = +5.0$ V \pm 10 % | (0.5 + a) T - 17 | | ns |
| | | | (0.5 + a) T - 40 | | ns |
| Address hold time (to ASTB↓) | thSTLA | $V_{DD} = +5.0$ V \pm 10 % | 0.5T - 24 | | ns |
| | | | 0.5T - 34 | | ns |
| Address hold time (to $\overline{RD}\uparrow$) | thRA | | 0.5T - 14 | | ns |
| Delay from address to $\overline{RD}\downarrow$ | tdAR | $V_{DD} = +5.0$ V \pm 10 % | (1 + a) T - 9 | | ns |
| | | | (1 + a) T - 15 | | ns |
| Address float time (to $\overline{RD}\downarrow$) | tfRA | | | 0 | ns |
| Delay from address to data input | tdAID | $V_{DD} = +5.0$ V \pm 10 % | | (2.5 + a + n) T - 37 | ns |
| | | | | (2.5 + a + n) T - 52 | ns |
| Delay from ASTB↓ to data input | tdSTID | $V_{DD} = +5.0$ V \pm 10 % | | (2 + n) T - 40 | ns |
| | | | | (2 + n) T - 60 | ns |
| Delay from $\overline{RD}\downarrow$ to data input | tdRID | $V_{DD} = +5.0$ V \pm 10 % | | (1.5 + n) T - 50 | ns |
| | | | | (1.5 + n) T - 70 | ns |
| Delay from ASTB↓ to $\overline{RD}\downarrow$ | tdSTR | | 0.5T - 9 | | ns |
| Data hold time (to $\overline{RD}\uparrow$) | thRID | | 0 | | ns |
| Delay from $\overline{RD}\uparrow$ to address active | tdRA | After program is read | $V_{DD} = +5.0$ V \pm 10 % | 0.5T - 8 | ns |
| | | | | 0.5T - 12 | ns |
| | | After data is read | $V_{DD} = +5.0$ V \pm 10 % | 1.5T - 8 | ns |
| | | | | 1.5T - 12 | ns |
| Delay from $\overline{RD}\uparrow$ to ASTB↑ | tdRST | | 0.5T - 17 | | ns |
| \overline{RD} low-level width | twRL | $V_{DD} = +5.0$ V \pm 10 % | (1.5 + n) T - 30 | | ns |
| | | | (1.5 + n) T - 40 | | ns |
| Address hold time (to $\overline{WR}\uparrow$) | thWA | | 0.5T - 14 | | ns |
| Delay from address to $\overline{WR}\downarrow$ | tdAW | $V_{DD} = +5.0$ V \pm 10 % | (1 + a) T - 5 | | ns |
| | | | (1 + a) T - 15 | | ns |
| Delay from ASTB↓ to data output | tdSTOD | $V_{DD} = +5.0$ V \pm 10 % | | 0.5T + 19 | ns |
| | | | | 0.5T + 35 | ns |
| Delay from $\overline{WR}\downarrow$ to data output | tdWOD | | | 0.5T - 11 | ns |
| Delay from ASTB↓ to $\overline{WR}\downarrow$ | tdSTW | | 0.5T - 9 | | ns |

Remarks T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states ($n \geq 0$)

(1) Read/write operation (2/2)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|-------------------|---------------------------------|------------------|------|------|
| Data setup time (to $\overline{WR}\uparrow$) | ts _{ODW} | V _{DD} = +5.0 V ± 10 % | (1.5 + n) T - 30 | | ns |
| | | | (1.5 + n) T - 40 | | ns |
| Data hold time (to $\overline{WR}\uparrow$) ^{Note} | t _{HWOD} | V _{DD} = +5.0 V ± 10 % | 0.5T - 5 | | ns |
| | | | 0.5T - 25 | | ns |
| Delay from $\overline{WR}\uparrow$ to $\overline{ASTB}\uparrow$ | t _{DWST} | | 0.5T - 12 | | ns |
| \overline{WR} low-level width | t _{WWL} | V _{DD} = +5.0 V ± 10 % | (1.5 + n) T - 30 | | ns |
| | | | (1.5 + n) T - 40 | | ns |

Note The hold time includes the time during which V_{OH1} and V_{OL1} are held under the load conditions of C_L = 50 pF and R_L = 4.7 kΩ.

Remarks T: T_{CYK} (system clock cycle time)
 n: Number of wait states (n ≥ 0)

(2) Bus hold timing

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|----------------------|---------------------------------|---------|--------------------|------|
| Delay from HLDRQ \uparrow to float | t _{FHQC} | | | (6 + a + n) T + 50 | ns |
| Delay from HLDRQ \uparrow to HLDAK \uparrow | t _{DHQHHAH} | V _{DD} = +5.0 V ± 10 % | | (7 + a + n) T + 30 | ns |
| | | | | (7 + a + n) T + 40 | ns |
| Delay from float to HLDAK \uparrow | t _{DCFHA} | | | 1T + 30 | ns |
| Delay from HLDRQ \downarrow to HLDAK \downarrow | t _{DHQLHAL} | V _{DD} = +5.0 V ± 10 % | | 2T + 40 | ns |
| | | | | 2T + 60 | ns |
| Delay from HLDAK \downarrow to active | t _{DHAC} | V _{DD} = +5.0 V ± 10 % | 1T - 20 | | ns |
| | | | 1T - 30 | | ns |

Remarks T: T_{CYK} (system clock cycle time)
 a: 1 (during address wait), otherwise, 0
 n: Number of wait states (n ≥ 0)

(3) External wait timing

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---------------------|--|--------------------|--------------------|------|
| Delay from address to $\overline{\text{WAIT}}\downarrow$ input | t_{DAWT} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $(2 + a) T - 40$ | ns |
| | | | | $(2 + a) T - 60$ | ns |
| Delay from $\text{ASTB}\downarrow$ to $\overline{\text{WAIT}}\downarrow$ input | t_{DSTWT} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $1.5T - 40$ | ns |
| | | | | $1.5T - 60$ | ns |
| Hold time from $\text{ASTB}\downarrow$ to $\overline{\text{WAIT}}$ | t_{HSTWTH} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | $(0.5 + n) T + 5$ | | ns |
| | | | $(0.5 + n) T + 10$ | | ns |
| Delay from $\text{ASTB}\downarrow$ to $\overline{\text{WAIT}}\uparrow$ | t_{DSTWTH} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $(1.5 + n) T - 40$ | ns |
| | | | | $(1.5 + n) T - 60$ | ns |
| Delay from $\overline{\text{RD}}\downarrow$ to $\overline{\text{WAIT}}\downarrow$ input | t_{DRWTL} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $T - 50$ | ns |
| | | | | $T - 70$ | ns |
| Hold time from $\overline{\text{RD}}\downarrow$ to $\overline{\text{WAIT}}\downarrow$ | t_{HRWT} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | $nT + 5$ | | ns |
| | | | $nT + 10$ | | ns |
| Delay from $\overline{\text{RD}}\downarrow$ to $\overline{\text{WAIT}}\uparrow$ | t_{DRWTH} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $(1 + n) T - 40$ | ns |
| | | | | $(1 + n) T - 60$ | ns |
| Delay from $\overline{\text{WAIT}}\uparrow$ to data input | t_{DWTID} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $0.5T - 5$ | ns |
| | | | | $0.5T - 10$ | ns |
| Delay from $\overline{\text{WAIT}}\uparrow$ to $\overline{\text{WR}}\uparrow$ | t_{DWTW} | | $0.5T$ | | ns |
| Delay from $\overline{\text{WAIT}}\uparrow$ to $\overline{\text{RD}}\uparrow$ | t_{DWTR} | | $0.5T$ | | ns |
| Delay from $\overline{\text{WR}}\downarrow$ to $\overline{\text{WAIT}}\downarrow$ input | t_{DWWTL} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $T - 50$ | ns |
| | | | | $T - 75$ | ns |
| Hold time from $\overline{\text{WR}}\downarrow$ to $\overline{\text{WAIT}}$ | t_{HWWT} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | $nT + 5$ | | ns |
| | | | $nT + 10$ | | ns |
| Delay from $\overline{\text{WR}}\downarrow$ to $\overline{\text{WAIT}}\uparrow$ | t_{DWWTH} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | | $(1 + n) T - 40$ | ns |
| | | | | $(1 + n) T - 70$ | ns |

Remarks T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states ($n \geq 0$)

(4) Refresh timing

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|--|---------------------|--|-------------|------|------|
| Random read/write cycle time | t_{RC} | | $3T$ | | ns |
| $\overline{\text{REFRQ}}$ low-level pulse width | t_{WRFQL} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | $1.5T - 25$ | | ns |
| | | | $1.5T - 30$ | | ns |
| Delay from $\text{ASTB}\downarrow$ to $\overline{\text{REFRQ}}$ | t_{DSTRFQ} | | $0.5T - 9$ | | ns |
| Delay from $\overline{\text{RD}}\uparrow$ to $\overline{\text{REFRQ}}$ | t_{DRRFQ} | | $1.5T - 9$ | | ns |
| Delay from $\overline{\text{WR}}\uparrow$ to $\overline{\text{REFRQ}}$ | t_{DWRFQ} | | $1.5T - 9$ | | ns |
| Delay from $\overline{\text{REFRQ}}\uparrow$ to ASTB | t_{DRFQST} | | $0.5T - 15$ | | ns |
| $\overline{\text{REFRQ}}$ high-level pulse width | t_{WRFQH} | $V_{\text{DD}} = +5.0 \text{ V} \pm 10 \%$ | $1.5T - 25$ | | ns |
| | | | $1.5T - 30$ | | ns |

Remark T: T_{CYK} (system clock cycle time)

SERIAL OPERATION ($T_A = -40$ to $+85$ °C, $V_{DD} = +2.7$ to 5.5 V, $AV_{SS} = V_{SS} = 0$ V)

(1) CSI

| Parameter | Symbol | Conditions | | MIN. | MAX. | Unit |
|---|--------------|---|---|-------------------|------------------|------|
| Serial clock cycle time ($\overline{SCK0}$) | t_{CYSK0} | Input | External clock When $\overline{SCK0}$ and $S00$ are CMOS I/O | $10/f_{XX} + 380$ | | ns |
| | | Output | | T | | μs |
| Serial clock low-level width ($\overline{SCK0}$) | t_{WSK0L} | Input | External clock When $\overline{SCK0}$ and $S00$ are CMOS I/O | $5/f_{XX} + 150$ | | ns |
| | | Output | | $0.5T - 40$ | | μs |
| Serial clock high-level width ($\overline{SCK0}$) | t_{WSK0H} | Input | External clock When $\overline{SCK0}$ and $S00$ are CMOS I/O | $5/f_{XX} + 150$ | | ns |
| | | Output | | $0.5T - 40$ | | μs |
| SIO setup time (to $\overline{SCK0}\uparrow$) | t_{SSSK0} | | | 40 | | ns |
| SIO hold time (to $\overline{SCK0}\uparrow$) | t_{HSSK0} | | | $5/f_{XX} + 40$ | | ns |
| S00 output delay time (to $\overline{SCK0}\downarrow$) | t_{DSBSK1} | CMOS push-pull output (3-wire serial I/O mode) | | 0 | $5/f_{XX} + 150$ | ns |
| | t_{DSBSK2} | Open-drain output (2-wire serial I/O mode), $R_L = 1$ kΩ | | 0 | $5/f_{XX} + 400$ | ns |

- Remarks**
1. The values in this table are those when C_L is 100 pF.
 2. T : Serial clock cycle set by software. The minimum value is $16/f_{XX}$.
 3. f_{XX} : Oscillator frequency

(2) IOE1, IOE2

| Parameter | Symbol | Conditions | | MIN. | MAX. | Unit |
|--|--------|--------------------------|---------------------------------|----------------|------|------|
| Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$) | tcYSK1 | Input | V _{DD} = +5.0 V ± 10 % | 250 | | ns |
| | | | | 500 | | ns |
| | Output | Internal, divided by 16 | T | | ns | |
| Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$) | tWSKL1 | Input | V _{DD} = +5.0 V ± 10 % | 85 | | ns |
| | | | | 210 | | ns |
| | Output | Internal, divided by 16 | 0.5T - 40 | | ns | |
| Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$) | tWSKH1 | Input | V _{DD} = +5.0 V ± 10 % | 85 | | ns |
| | | | | 210 | | ns |
| | Output | Internal, divided by 16 | 0.5T - 40 | | ns | |
| Setup time for SI1 and SI2 (to $\overline{SCK1}$, $\overline{SCK2}\uparrow$) | tSSK1 | | | 40 | | ns |
| Hold time for SI1 and SI2 (to $\overline{SCK1}$, $\overline{SCK2}\uparrow$) | tHSSK1 | | | 40 | | ns |
| Output delay time for SO1 and SO2 (to $\overline{SCK1}$, $\overline{SCK2}\downarrow$) | tDSOSK | | | 0 | 50 | ns |
| Output hold time for SO1 and SO2 (to $\overline{SCK1}$, $\overline{SCK2}\uparrow$) | tHSOSK | When data is transferred | | 0.5tcYSK1 - 40 | | ns |

Remarks 1. The values in this table are those when C_L is 100 pF.

2. T: Serial clock cycle set by software. The minimum value is 16/f_{xx}.

(3) UART, UART2

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|-----------------------------|--------|---------------------------------|------|------|------|
| ASCK clock input cycle time | tcYASK | V _{DD} = +5.0 V ± 10 % | 125 | | ns |
| | | | 250 | | ns |
| ASCK clock low-level width | tWASKL | V _{DD} = +5.0 V ± 10 % | 52.5 | | ns |
| | | | 85 | | ns |
| ASCK clock high-level width | tWASKH | V _{DD} = +5.0 V ± 10 % | 52.5 | | ns |
| | | | 85 | | ns |

OTHER OPERATIONS

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|--------------------|------------|--------------------------|------|------|
| NMI low-level width | t _{WNIL} | | 10 | | μs |
| NMI high-level width | t _{WNIH} | | 10 | | μs |
| INTP0 low-level width | t _{WIT0L} | | 3t _{CYSMP} + 10 | | ns |
| INTP0 high-level width | t _{WIT0H} | | 3t _{CYSMP} + 10 | | ns |
| Low-level width for INTP1-INTP3 and CI | t _{WIT1L} | | 3t _{CYCPU} + 10 | | ns |
| High-level width for INTP1-INTP3 and CI | t _{WIT1H} | | 3t _{CYCPU} + 10 | | ns |
| Low-level width for INTP4 and INTP5 | t _{WIT2L} | | 10 | | μs |
| High-level width for INTP4 and INTP5 | t _{WIT2H} | | 10 | | μs |
| RESET low-level width | t _{WRSL} | | 10 | | μs |
| RESET high-level width | t _{WRSH} | | 10 | | μs |

Remarks t_{CYSMP}: Sampling clock set by software
t_{CYCPU}: CPU operation clock set by software in the CPU

A/D CONVERTER CHARACTERISTICS

(T_A = -40 to +85 °C, V_{DD} = AV_{DD} = AV_{REF1} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------------|-------------------|----------------------------------|------|-------|--------------------------|------------------|
| Resolution | | | 8 | | | bit |
| Total error ^{Note} | | | | | 1.0 | % |
| Linearity calibration ^{Note} | | | | | 0.8 | % |
| Quantization error | | | | | ±1/2 | LSB |
| Conversion time | t _{CONV} | FR = 1 | 120 | | | t _{CYK} |
| | | FR = 0 | 180 | | | t _{CYK} |
| Sampling time | t _{SAMP} | FR = 1 | 24 | | | t _{CYK} |
| | | FR = 0 | 36 | | | t _{CYK} |
| Analog input voltage | V _{IAN} | | -0.3 | | AV _{REF1} + 0.3 | V |
| Analog input impedance | R _{AN} | | | 1 000 | | MΩ |
| AV _{REF1} current | I _{REF1} | | | 0.5 | 1.5 | mA |
| AV _{DD} supply current | I _{DD1} | f _{XX} = 32 MHz, CS = 1 | | 2.0 | 5.0 | mA |
| | I _{DD2} | STOP mode, CS = 0 | | 1.0 | 20 | μA |

Note Quantization error is not included. This parameter is indicated as the ratio to the full-scale value.

Remark t_{CYK}: System clock cycle time

D/A CONVERTER CHARACTERISTICS ($T_A = -40$ to $+85$ °C, $V_{DD} = AV_{DD} = +2.7$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V)

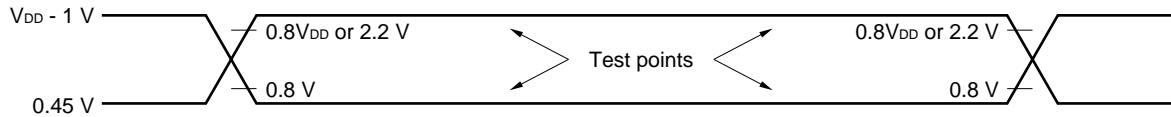
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|-------------|---------------------------------|--|------|--------------|------|---|
| Resolution | | | 8 | | | bit | |
| Total error | | Load conditions: 4 MΩ, 30 pF | $V_{DD} = AV_{DD} = AV_{REF2} = +2.7$ to 5.5 V $AV_{REF3} = 0$ V | | | 0.6 | % |
| | | | $V_{DD} = AV_{DD} = +2.7$ to 5.5 V $AV_{REF2} = 0.75V_{DD}$ $AV_{REF3} = 0.25V_{DD}$ | | | 0.8 | % |
| | | Load conditions: 2 MΩ, 30 pF | $V_{DD} = AV_{DD} = AV_{REF2} = +2.72.7$ to 5.5 V $AV_{REF3} = 0$ V | | | 0.8 | % |
| | | | $V_{DD} = AV_{DD} = +2.7$ to 5.5 V $AV_{REF2} = 0.75V_{DD}$ $AV_{REF3} = 0.25V_{DD}$ | | | 1.0 | % |
| Settling time | | Load conditions: 2 MΩ, 30 pF | | | 10 | μs | |
| Output resistance | R_o | DACS0, 1 = 55 H | | 10 | | kΩ | |
| Analog reference voltage | AV_{REF2} | | $0.75V_{DD}$ | | V_{DD} | V | |
| | AV_{REF3} | | 0 | | $0.25V_{DD}$ | V | |
| Resistance of AV_{REF2} and AV_{REF3} | R_{AIREF} | DACS0, 1 = 55 H | 4 | 8 | | kΩ | |
| Reference power supply input current | AI_{REF2} | | 0 | | 5 | mA | |
| | AI_{REF3} | | -5 | | 0 | mA | |

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|-----------------------------------|----------------------|------|----------------------|------|
| Data retention voltage | V _{DDDR} | STOP mode | 2.5 | | 5.5 | V |
| Data retention current | I _{DDDR} | V _{DDDR} = +2.7 to 5.5 V | | 10 | 50 | μA |
| | | V _{DDDR} = +2.5 V | | 2 | 10 | μA |
| V _{DD} rise time | t _{rVD} | | 200 | | | μs |
| V _{DD} fall time | t _{fVD} | | 200 | | | μs |
| V _{DD} hold time (to STOP mode setting) | t _{HVD} | | 0 | | | ms |
| STOP clear signal input time | t _{DREL} | | 0 | | | ms |
| Oscillation settling time | t _{WAIT} | Crystal | 30 | | | ms |
| | | Ceramic resonator | 5 | | | ms |
| Input low voltage | V _{IL} | Specific pins ^{Note} | 0 | | 0.1V _{DDDR} | V |
| Input high voltage | V _{IH} | | 0.9V _{DDDR} | | V _{DDDR} | V |

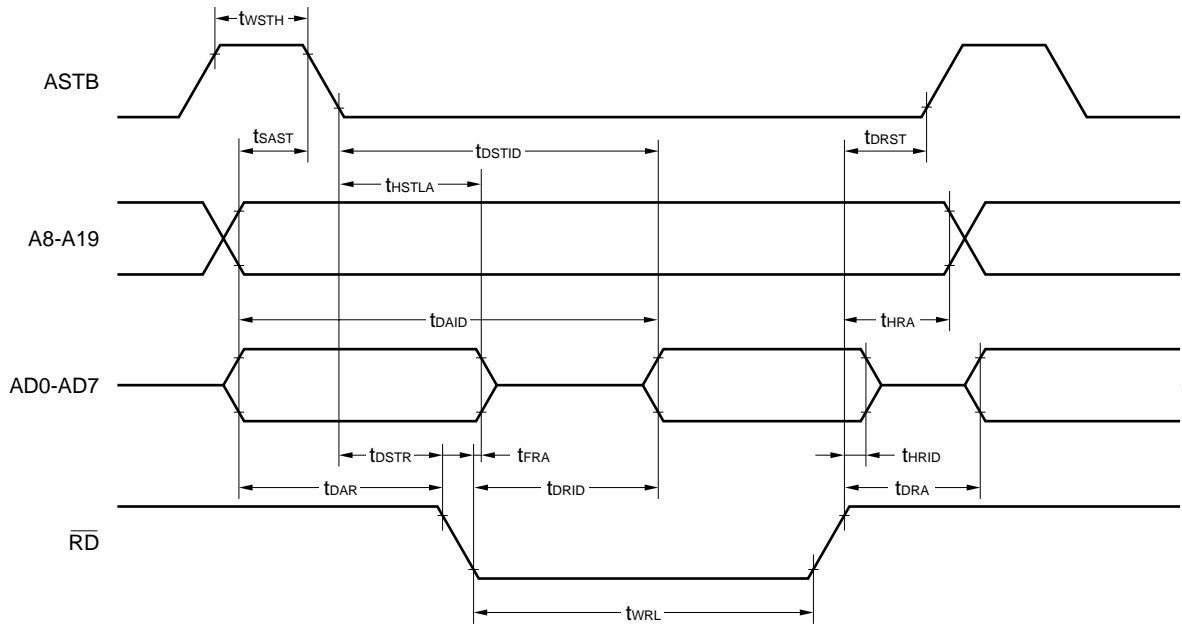
Note $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/SCK1, P26/INTP5, P27/SI0, P32/ $\overline{\text{SCK0}}$ /SCL, and P33/SO0/SDA pins

AC TIMING TEST POINTS

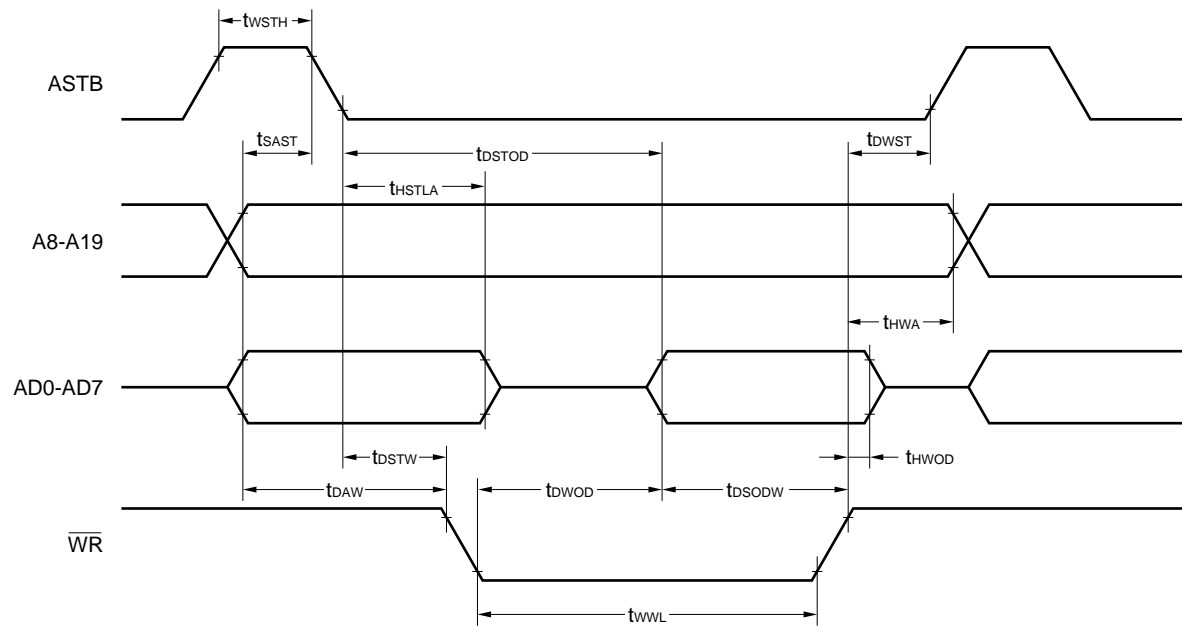


TIMING WAVEFORM

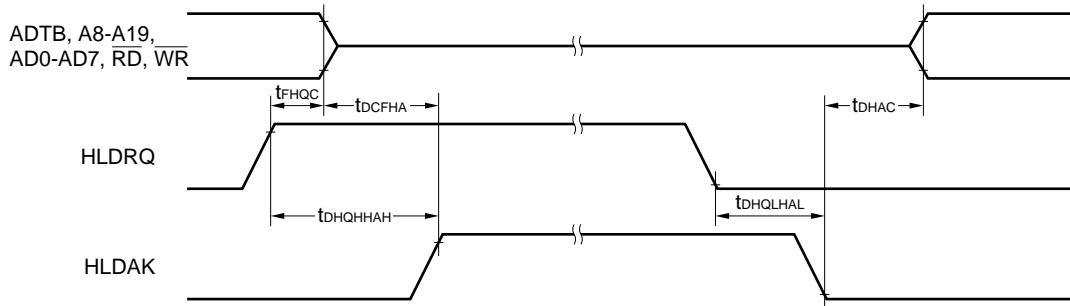
(1) Read operation



(2) Write operation

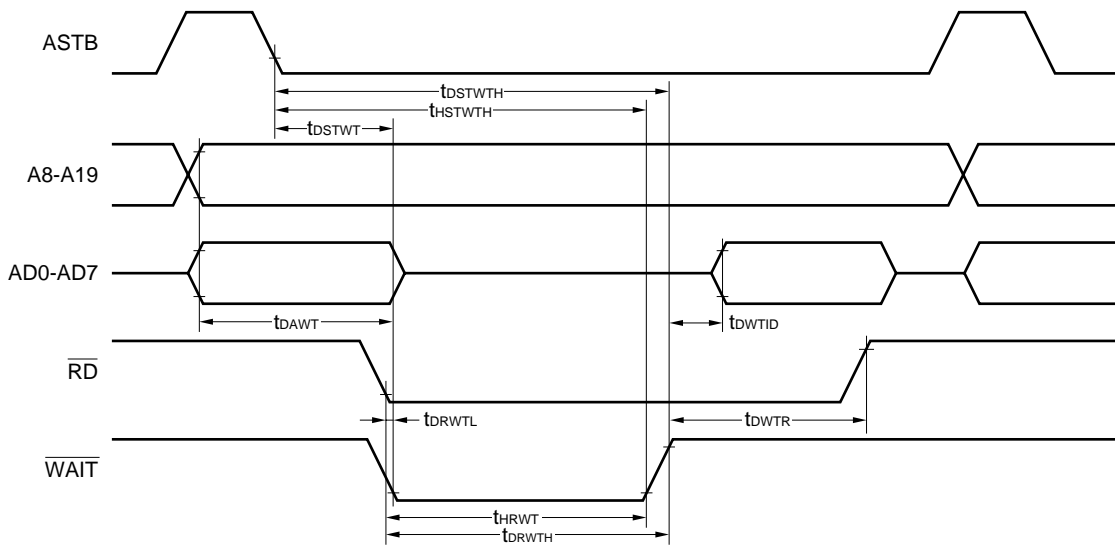


HOLD TIMING

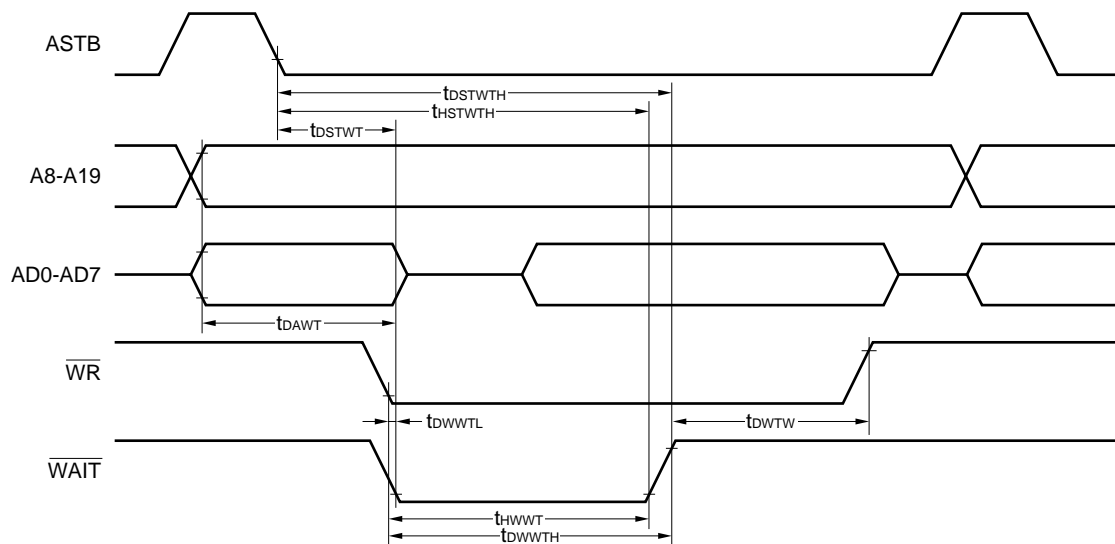


EXTERNAL WAIT SIGNAL INPUT TIMING

(1) Read operation

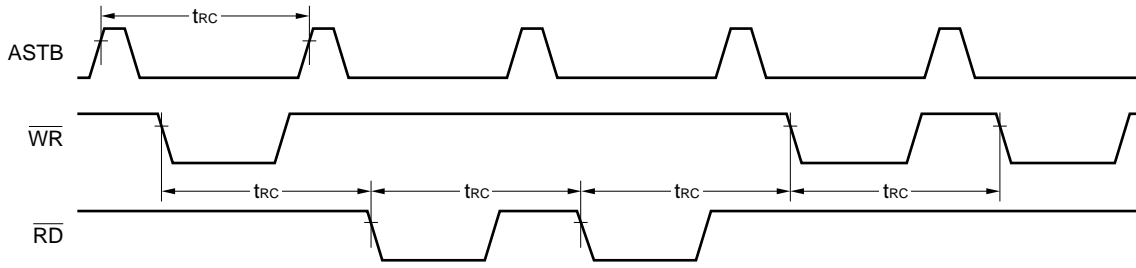


(2) Write operation

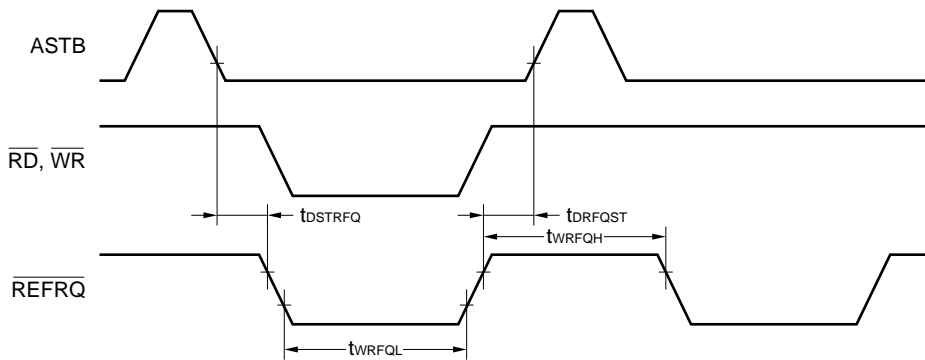


REFRESH TIMING WAVEFORM

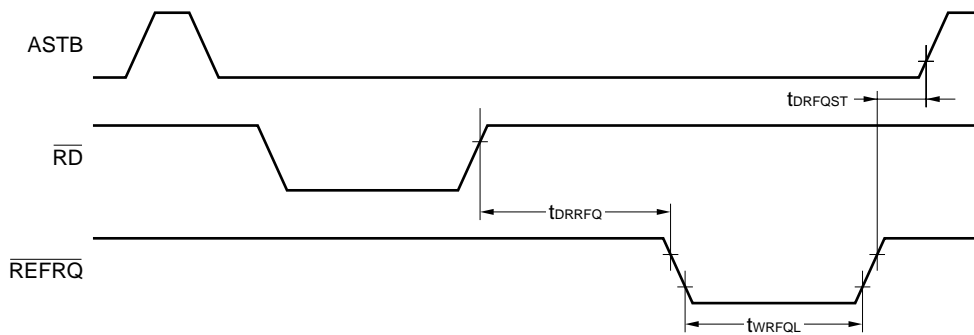
(1) Random read/write cycle



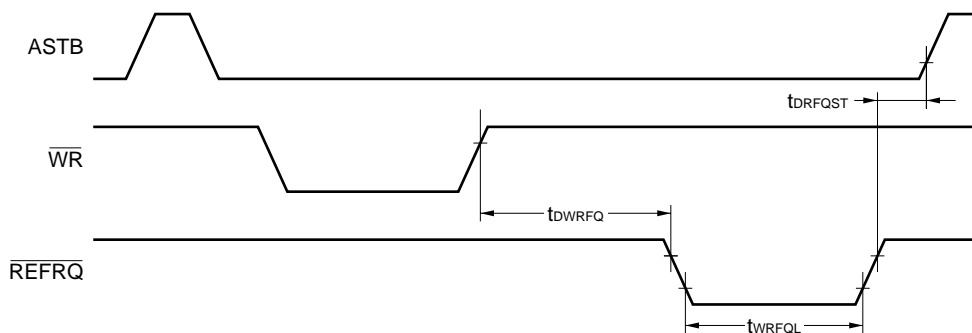
(2) When refresh memory is accessed for a read and write at the same time



(3) Refresh after a read

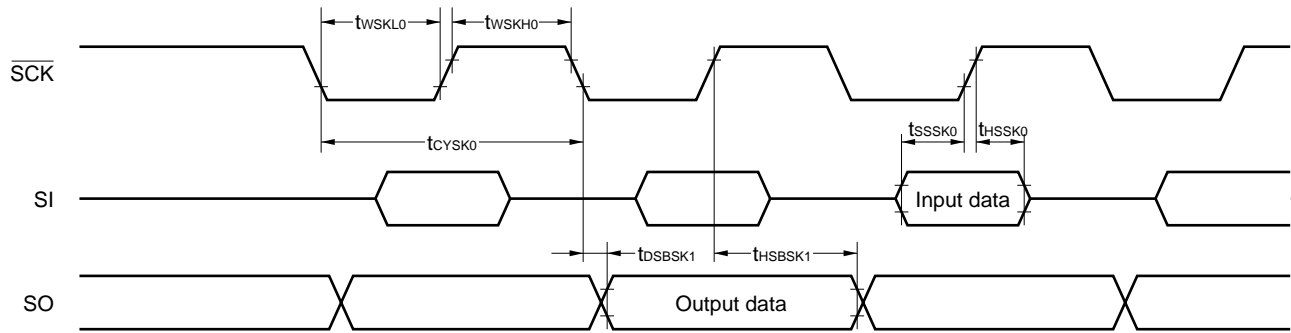


(4) Refresh after a write

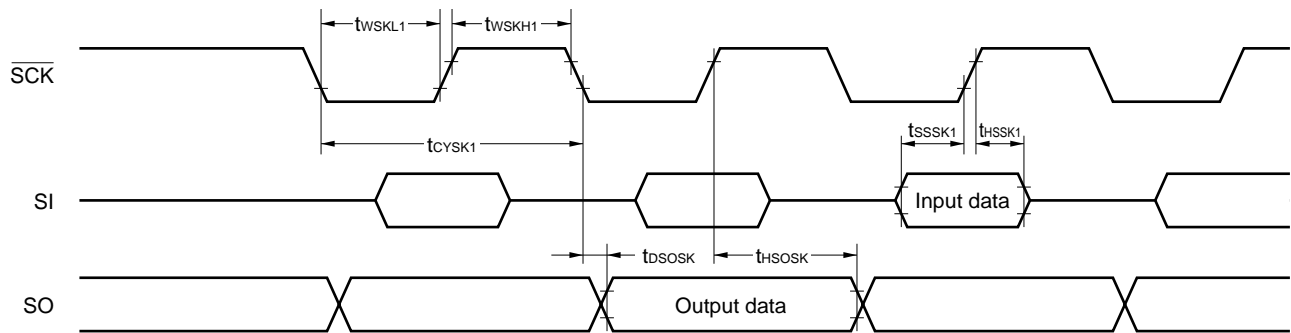


SERIAL OPERATION

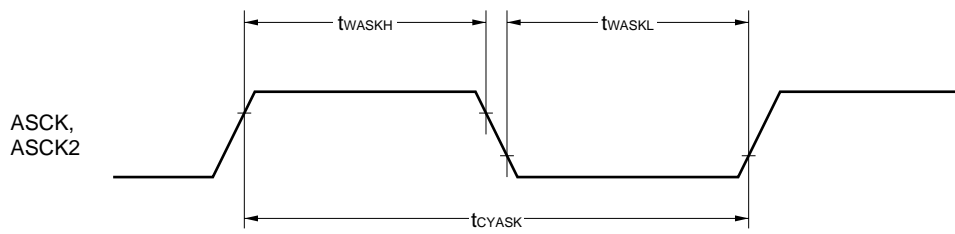
(1) CSI



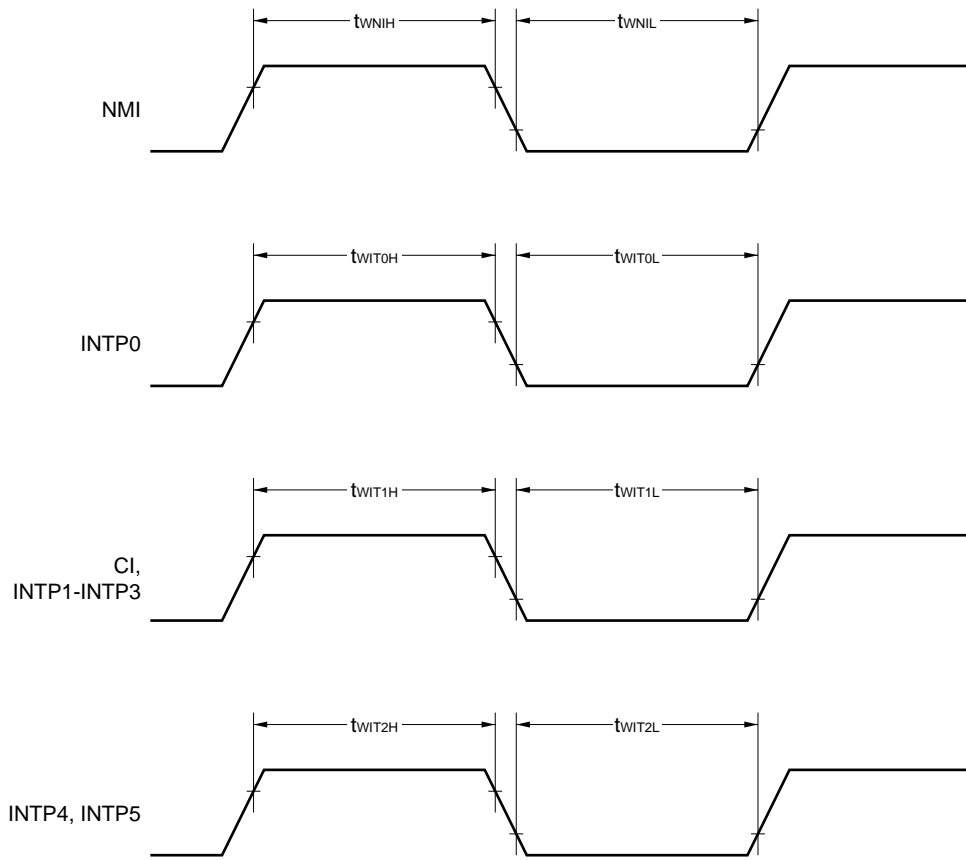
(2) IOE1, IOE2



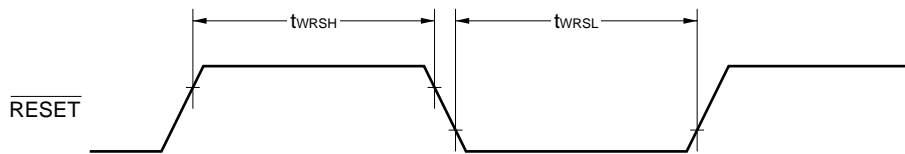
(3) UART, UART2



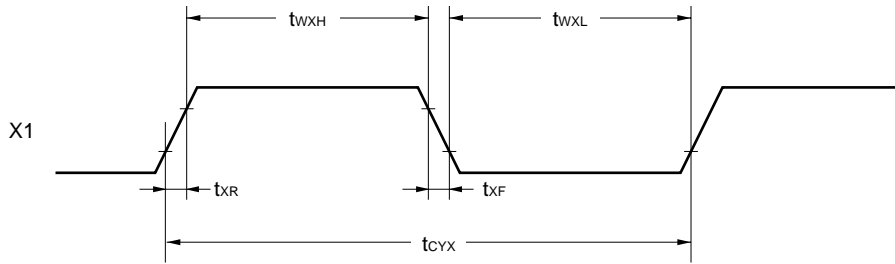
INTERRUPT INPUT TIMING



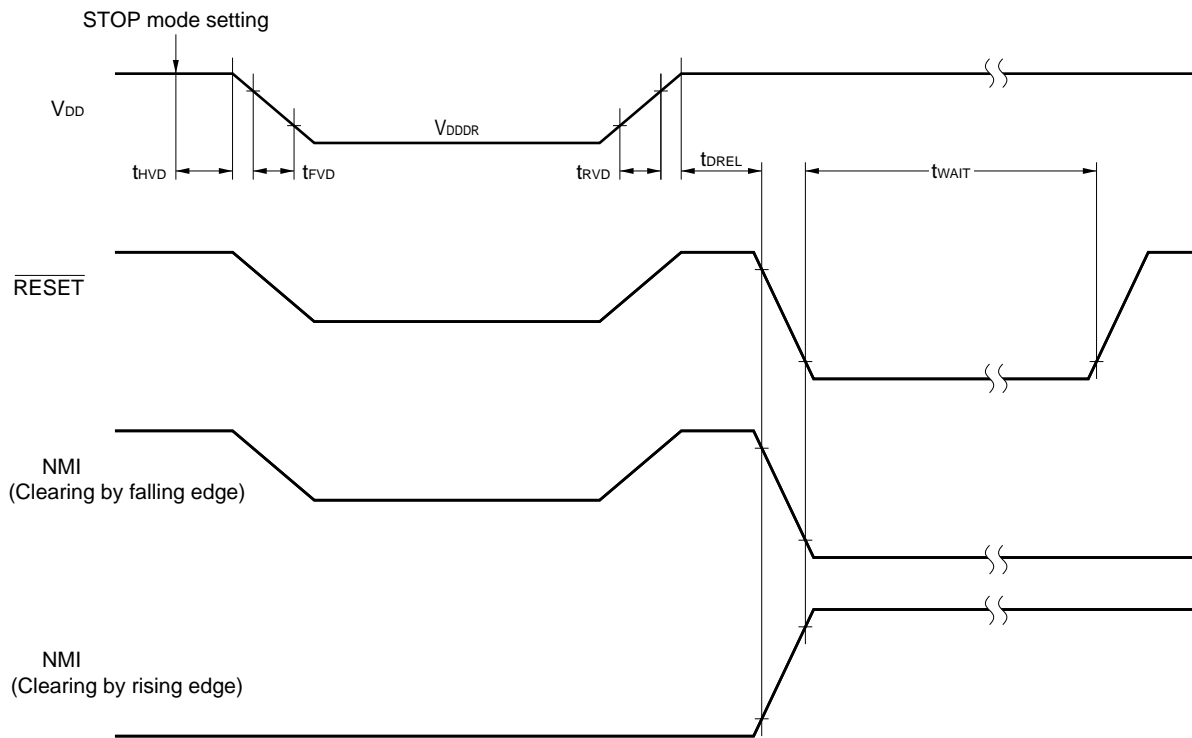
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

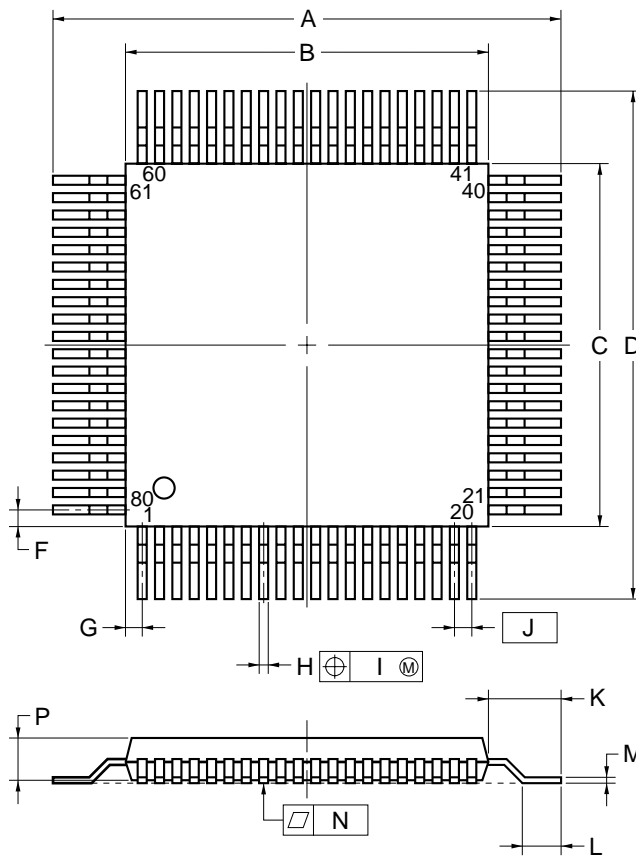


DATA RETENTION CHARACTERISTICS

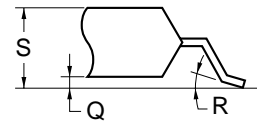


15. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

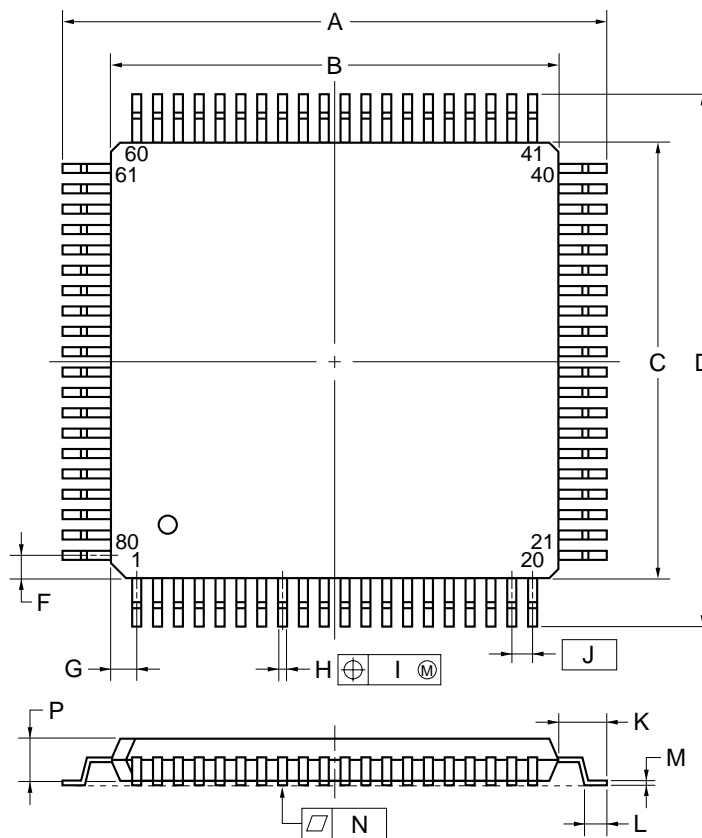
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 17.2±0.4 | 0.677±0.016 |
| B | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| C | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.2±0.4 | 0.677±0.016 |
| F | 0.825 | 0.032 |
| G | 0.825 | 0.032 |
| H | 0.30±0.10 | 0.012 ^{+0.004} _{-0.005} |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.6±0.2 | 0.063±0.008 |
| L | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.15 ^{+0.10} _{-0.05} | 0.006 ^{+0.004} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 2.7 | 0.106 |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |

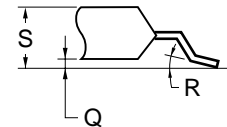
S80GC-65-3B9-4

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

★ 80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

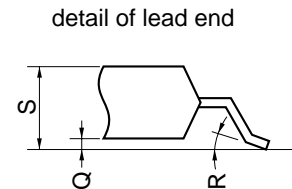
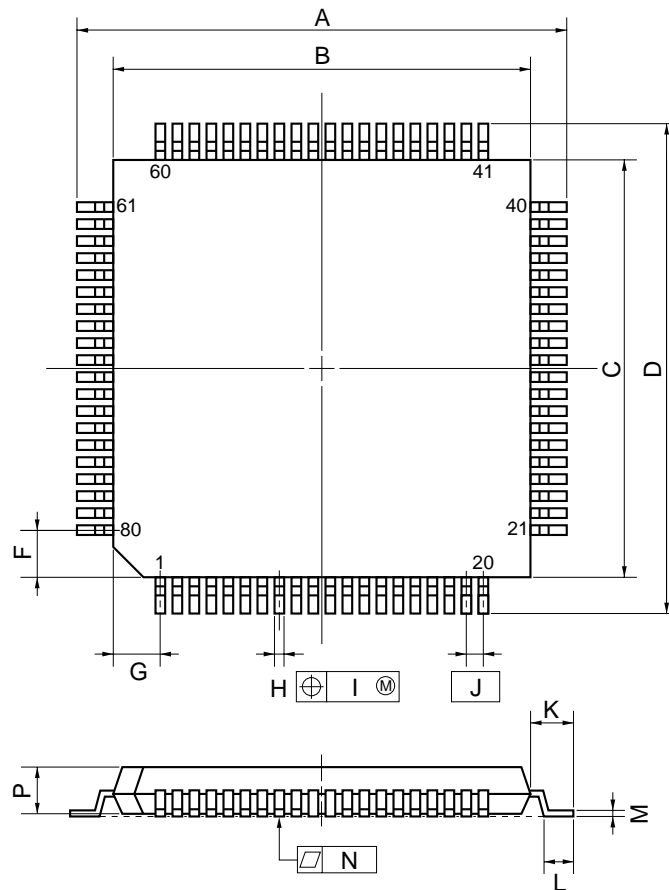
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 17.20±0.20 | 0.677±0.008 |
| B | 14.00±0.20 | 0.551 ^{+0.009} _{-0.008} |
| C | 14.00±0.20 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.20±0.20 | 0.677±0.008 |
| F | 0.825 | 0.032 |
| G | 0.825 | 0.032 |
| H | 0.32±0.06 | 0.013 ^{+0.002} _{-0.003} |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.60±0.20 | 0.063±0.008 |
| L | 0.80±0.20 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.17 ^{+0.03} _{-0.07} | 0.007 ^{+0.001} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 1.40±0.10 | 0.055±0.004 |
| Q | 0.125±0.075 | 0.005±0.003 |
| R | 3° ^{+7°} _{-3°} | 3° ^{+7°} _{-3°} |
| S | 1.70 MAX. | 0.067 MAX. |

P80GC-65-8BT

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| B | 12.0±0.2 | 0.472 ^{+0.009} _{-0.008} |
| C | 12.0±0.2 | 0.472 ^{+0.009} _{-0.008} |
| D | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| F | 1.25 | 0.049 |
| G | 1.25 | 0.049 |
| H | 0.22 ^{+0.05} _{-0.04} | 0.009±0.002 |
| I | 0.10 | 0.004 |
| J | 0.5 (T.P.) | 0.020 (T.P.) |
| K | 1.0±0.2 | 0.039 ^{+0.009} _{-0.008} |
| L | 0.5±0.2 | 0.020 ^{+0.008} _{-0.009} |
| M | 0.145 ^{+0.055} _{-0.045} | 0.006±0.002 |
| N | 0.10 | 0.004 |
| P | 1.05 | 0.041 |
| Q | 0.05±0.05 | 0.002±0.002 |
| R | 5°±5° | 5°±5° |
| S | 1.27 MAX. | 0.050 MAX. |

P80GK-50-BE9-4

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

★ 16. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD784031.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 16-1. Soldering Conditions for Surface-Mount Devices (1/2)

(1) μPD784031GC-3B9: 80-pin plastic QFP (14 × 14 × 2.7 mm)

| Soldering process | Soldering conditions | Symbol |
|------------------------|--|-----------|
| Infrared ray reflow | Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 3 | IR35-00-3 |
| VPS | Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 3 | VP15-00-3 |
| Wave soldering | Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120 °C max. (measured on the package surface) | WS60-00-1 |
| Partial heating method | Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device) | - |

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

(2) μPD784031GC-8BT: 80-pin plastic QFP (14 × 14 × 1.4 mm)

| Soldering process | Soldering conditions | Symbol |
|------------------------|--|-----------|
| Infrared ray reflow | Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 2 | IR35-00-2 |
| VPS | Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 2 | VP15-00-2 |
| Wave soldering | Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120 °C max. (measured on the package surface) | WS60-00-1 |
| Partial heating method | Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device) | - |

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

Table 16-1. Soldering Conditions for Surface-Mount Devices (2/2)

(3) μPD784031GK-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

| Soldering process | Soldering conditions | Symbol |
|------------------------|---|------------|
| Infrared ray reflow | Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days ^{Note} (10 hours of pre-baking is required at 125 °C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking. | IR35-107-2 |
| VPS | Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days ^{Note} (10 hours of pre-baking is required at 125 °C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking. | VP15-107-2 |
| Partial heating method | Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device) | - |

Note Maximum number of days during which the product can be stored at a temperature of 25 °C and a relative humidity of 65 % or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μ PD784031.

Language Processing Software

| | |
|----------------------------|---|
| RA78K4 ^{Note 1} | Assembler package for all 78K/IV series models |
| CC78K4 ^{Note 1} | C compiler package for all 78K/IV series models |
| CC78K4-L ^{Note 1} | C compiler library source file for all 78K/IV series models |

PROM Write Tools

| | |
|--|---|
| PG-1500 | PROM programmer |
| PA-78P4026GC PA-78P4038GK PA-78P4026KK | Programmer adaptor, connects to PG-1500 |
| PG-1500 controller ^{Note 2} | Control program for PG-1500 |

Debugging Tools

| | |
|-----------------------------------|--|
| IE-784000-R | In-circuit emulator for all 78K/IV sub-series models |
| IE-784000-R-BK | Break board for all 78K/IV series models |
| IE-784038-R-EM1 IE-784000-R-EM | Emulation board for evaluating μ PD784038 sub-series models |
| IE-70000-98-IF-B | Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine |
| IE-70000-98N-IF | Interface adapter and cable when a PC-9800 series notebook is used as the host machine |
| IE-70000-PC-IF-B | Interface adapter when the IBM PC/AT™ is used as the host machine |
| IE-78000-R-SV3 | Interface adapter and cable when the EWS is used as the host machine |
| EP-78230GC-R | Emulation probe for 80-pin plastic QFP (GC-3B9 and GC-8BT types) for all μ PD784038 sub-series |
| EP-78054GK-R | Emulation probe for 80-pin plastic TQFP (fine pitch) (GK-BE9 type) for all μ PD784038 sub-series |
| EV-9200GC-80 | Socket for mounting on target system board made for 80-pin plastic QFP (GC-3B9 and GC-8BT types) |
| TGK-080SDW | Adapter for mounting on target system board made for 80-pin plastic TQFP (fine pitch) (GK-BE9 type) |
| EV-9900 | Tool used to remove the μ PD78P4038KK-T from the EV-9200GC-80 |
| SM78K4 ^{Note 3} | System simulator for all 78K/IV series models |
| ID78K4 ^{Note 3} | Integrated debugger for IE-784000-R |
| DF784038 ^{Note 4} | Device file for all μ PD784038 sub-series models |

Real-Time OS

| | |
|----------------------------|---------------------------------------|
| RX78K/IV ^{Note 4} | Real-time OS for 78K/IV series models |
| MX78K4 ^{Note 2} | OS for all 78K/IV series models |

- Notes 1.**
- Based on PC-9800 series (MS-DOST™)
 - Based on IBM PC/AT and compatibles (PC DOST™, Windows™, MS-DOS, and IBM DOST™)
 - Based on HP9000 series 700™ (HP-UXT™)
 - Based on SPARCstation™ (SunOST™)
 - Based on NEWST™ (NEWS-OST™)
- 2.**
- Based on PC-9800 series (MS-DOS)
 - Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
- 3.**
- Based on PC-9800 series (MS-DOS + Windows)
 - Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
 - Based on HP9000 series 700 (HP-UX)
 - Based on SPARCstation (SunOS)
- 4.**
- Based on PC-9800 series (MS-DOS)
 - Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
 - Based on HP9000 series 700 (HP-UX)
 - Based on SPARCstation (SunOS)

- Remarks 1.** The RA78K4, CC78K4, SM78K4, and ID78K4 are used with the DF784038.
- 2.** The TGK-080SDW is a product of TOKYO ELETECH CORPORATION (Tokyo, 03-5295-1661). Consult the NEC sales representative for purchasing.

APPENDIX B RELATED DOCUMENTS

Documents Related to Devices

| Document name | Document No. | |
|---|--------------|-------------|
| | Japanese | English |
| μPD784031 Data Sheet | U11507J | This manual |
| μPD784035, 784036, 784037, 784038 Data Sheet | U10847J | U10847E |
| μPD78P4038 Data Sheet | U10848J | U10848E |
| μPD784038, 784038Y Sub-Series User's Manual, Hardware | U11316J | U11316E |
| μPD784038 Sub-Series Special Function Registers | U11090J | - |
| 78K/IV Series User's Manual, Instruction | U10905J | U10905E |
| 78K/IV Series Instruction Summary Sheet | U10594J | - |
| 78K/IV Series Instruction Set | U10595J | - |
| 78K/IV Series Application Note, Software Basic | U10095J | - |

Documents Related to Development Tools (User's Manual)

| Document name | | Document No. | |
|---|---|--------------|----------|
| | | Japanese | English |
| RA78K4 Assembler Package | Operation | U11334J | U11334E |
| | Language | U11162J | - |
| RA78K Series Structured Assembler Preprocessor | | EEU-817 | EEU-1402 |
| CC78K4 Series | Operation | EEU-960 | - |
| | Language | EEU-961 | - |
| CC78K Series Library Source File | | EEU-777 | - |
| PG-1500 PROM Programmer | | EEU-651 | EEU-1335 |
| PG-1500 Controller PC-9800 Series (MS-DOS) Base | | EEU-704 | EEU-1291 |
| PG-1500 Controller IBM PC Series (PC DOS) Base | | EEU-5008 | U10540E |
| IE-784000-R | | EEU-5004 | EEU-1534 |
| IE-784038-R-EM1 | | U11383J | U11383E |
| EP-78230 | | EEU-985 | EEU-1515 |
| EP-78054GK-R | | EEU-932 | EEU-1468 |
| SM78K4 System Simulator Windows Base | Reference | U10093J | U10093E |
| SM78K Series System Simulator | External Parts User Open Interface Specifications | U10092J | U10092E |
| ID78K4 Integrated Debugger Windows Base | Reference | U10440J | U10440E |

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

Documents Related to Software to Be Incorporated into the Product (User's Manual)

| Document name | | Document No. | |
|-----------------------------|--------------|--------------|---------|
| | | Japanese | English |
| 78K/IV Series Real-Time OS | Basic | U10603J | - |
| | Installation | U10604J | - |
| | Debugger | U10364J | - |
| OS for 78K/IV Series MX78K4 | Basic | U11779J | - |

Other Documents

| Document name | Document No. | |
|---|--------------|----------|
| | Japanese | English |
| IC PACKAGE MANUAL | C10943X | |
| SMD Surface Mount Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Device | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Electrostatic Discharge (ESD) Test | MEM-539 | - |
| Guide to Quality Assurance for Semiconductor Device | C11893J | MEI-1202 |
| Guide for Products Related to Micro-Computer: Other Companies | C11416J | - |

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Network requirements

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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